Prime Computer Logic Diagrams

STORAGE MODULE CONTROLLER
W.W. / E.V.

LOGIC DIAG. LDS 2523

Prime Computer, Incorporated, 145 Pennsylvania Avenue, Framingham, Massachusetts 01701

TABLE OF CONTENTS

STORAGE MODULE CONTROLLER
W.W. / E.V.

LOGIC DIAG. LDS 2523

DWG NO.	DATE	REV
LDS 2523	4 15 77	A

PE-T-221 Rev 1	LTR	DATE	REVISION	DR.	CK.

MATERIAL	DWN	PRIME COMPUTER INC. NATICK, MASS.			
	CHK				
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES –DIMENSIONS ARE IN INCHES –TOLERANCES xx ±.02 xxx ±.005 ANGLES ±1/2°	ENG. D. Gardiner	Storage Module Controller			
	APPRD				
	USED ON	SCALE	SIZE	DWG. NO.	REV.
	NEXT ASSY	SHEET 1 OF 24		SPC 2466	1

I-01

DATE: May 21, 1976

TO: Programming and Engineering Staff

FROM: Derek J. Gardiner

SUBJECT: Storage Module Controller Specification

Now available from Drafting is Rev 1 of the Storage Module Specification SPC 2466. Major differences are as follows:

1) Dual port devices described in paragraph 2.4.

2) Data field checkword doubled in size to 32 bits to allow error correction as well as detection.

3) Table 1 revised to make the standard record size 1040 words instead of 1032.

4) Extra INA added - input OAR.

5) Mask field expanded from five to six bits to assist dual port operation.

6) Select order changed to allow a "de-select".

7) Seek order to current track no longer takes any appreciable time.

8) Status bit 11 added for dual-port operation.

9) Use of "short-read" feature clarified.

10) Inter-record channel processing time extended.

11) Appendix A added to explain the error correction process.

Derek Gardiner

Derek J. Gardiner
/nf

Also see "NOTE" on the following page.

NOTE: The following products are released and available.

Prime No.	Description
4240	One 80 megabyte storage module, controller, one pack, cables.
4241	One 80 megabyte storage module, with pack, to add to 4240 or 4242.
4242	One 300 megabyte storage module, controller, one pack, cables.
4243	One 300 megabyte storage module, with pack, to add to 4240 or 4242.

Dual port devices are not yet available. The controller is not available by itself.

LTR	DATE	REVISION	DR.	CK.

1.0 GENERAL

This specification describes the operating characteristics of model 4004 disk controller. This controller interfaces to CDC "Storage Module" diskfiles. These are high capacity, high transfer rate devices which store data on special disk packs with platters similar to IBM 3330. Up to four Storage Module devices may be used on one controller. Minimum on-line storage is 80 megabytes of data; maximum is 1200 megabytes. Two controllers are supported by software.

The Storage Module Controller (SMC), designated Prime model number 4004, is not program compatible with other disk controllers in the Prime model line. Storage module media is neither mechanically nor format compatible with other Prime diskfiles. This controller requires that the Prime CPU be equipped with DMT. It is a software requirement that the CPU have high-speed arithmetic. This controller receives its orders as a channel processor in a manner similar to Prime models 4001/2/3. DMT is needed for this. Note: "Words" in this specification are defined to be 16 bits long.

2.0 OVERALL CHARACTERISTICS

2.1 Data Organization

Data on the disk is organized in cylinders, tracks and records. A given recording surface is divided into concentric circles defined as tracks. Each track is subdivided into records. A recording area accessible without head movement on one spindle is defined as a cylinder. A five-surface disk pack has 5 tracks per cylinder and a 19 surface disk pack has 19 tracks per cylinder. Each cylinder can have up to 19 read/write heads. These heads can be positioned in any one of 823 positions (tracks).

2.2 Device Specifications

Storage Module devices have either a five platter disk pack or a twelve platter disk pack. These give an unformatted capacity of about 80 and 300 megabytes of storage. Device parameters are as follows:

	80 Megabyte	300 Megabyte
Speed (RPM)	3600	3600
Recording density (bpi)	6038	6038
Bits/tracks	161280	161280
Tracks/disk	823	823
Track density (tpi)	400	400
Platters	5	12
Data surfaces	5	19
Data rate (MHz)	9.67	9.67
Seek time, one track (ms)	6	6
Seek time, 823 tracks (ms)	55	55

	80 Megabyte	300 Megabyte
Weight (lbs.)		
Rack mounted device	165	-
Base cabineted device	213	600
Voltage/frequency	120/60Hz	208/60Hz
	220/50Hz	220/50Hz

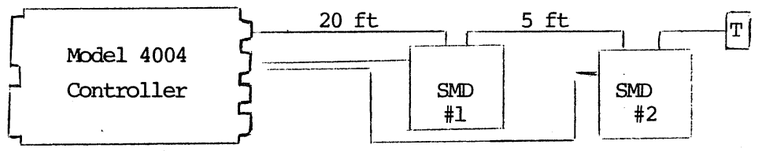
These diskfiles use one complete platter as a servo-surface. This is how they can achieve a track density of 400 tpi and still guarantee media interchangeability between drives. Note: 80 megabyte diskpacks cannot be used in the 300 megabyte drive.

The 80 megabyte diskfile can be rack mounted or supplied on a base cabinet; the latter is available in two styles (and prices) - utilitarian and deluxe. Two 80 megabyte files can be mounted in the deluxe cabinet.

Each diskfile has an operator panel with three indicators/switches: Start, Ready, Fault.

2.3 Device Cabling

Cables between the controller and the storage module devices are part daisy-chain, part radial. The figure below shows how this is arranged.



The interface between model 4004 and the storage modules uses differential drivers and receivers. The last device in the daisy chain has a terminator.

2.4 Dual Port Devices

Storage Modules are available with a dual-port capability such that two controllers may have access to a single device. Figure 1 shows a configuration with CPU number 1 having exclusive access to an 80 megabyte device and shared access to two 300 megabyte devices. CPU number 2 has exclusive access to one 80 and one 300 megabyte device plus shared access to the same two 300 megabyte devices.

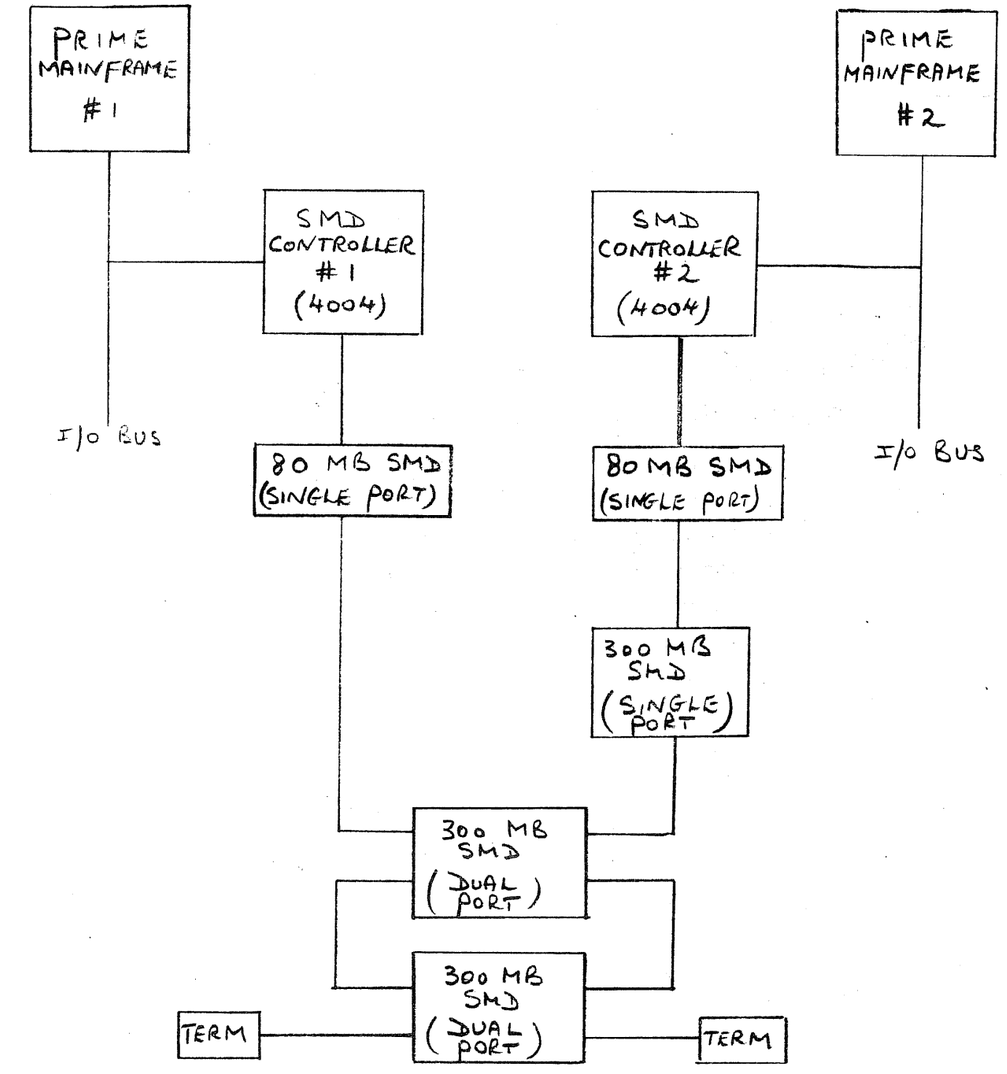


FIGURE 1. DUAL-PORT CAPABILITY

2.5 Record Layout

Each track on each disk surface will store about 10,000 computer words. As this is an inconveniently large chunk to read or write at any one time, the surface of the disk is divided into records. As each record (regardless of its size) requires a fixed overhead of words to be recorded for control purposes, the smaller the record size, the greater the wastage of storage space. This controller utilizes a flexible record arrangement. The size of the record is determined at the time the diskpack is "formatted". It is customary to use the same format for the complete disk, but this is not a requirement as far as the controller is concerned. The controller requires only that each track have equal length records.

2.6 Recording Format

In addition to the actual data, each record contains other fields used for synchronization, circuit recovery times, data error checking and head and track integrity checking. The latter is a 48 bit field recorded on the disk ahead of each data field - the recording is done during a pack format operation and normally would be done once only for the life of the pack. This field is known as a header. The information recorded in each header is unique for each data field on the diskpack. Each time an access is made to a specific data field on a diskpack, a check is made that the expected header agrees with the actual header.

Each record will have the following fields.

Field	Size and Content
Address mark	24 bits of erase
Sync No. 1	216 zeros
Flag No. 1	8 ones
Header	48 bits
Head gap	4 zeros
Sync No. 2	204 zeros
Flag No. 2	8 ones
Data field	(32 x 16) bits minimum
	(2048 x 16) bits maximum
Checkword	32 bits
Postamble	736 zeros

All the above fields, with the exception of the data field, constitute a fixed overhead of 1280 bits per record. The address mark field is a special synchronizing flag which alerts the controller that a header field is about to be read. The postamble is a field which is used as a space between records to allow channel processing to take place from one read/write order to the next. This is explained in detail in paragraph 3.7 below.

2.7 Storage Capacity

The storage capacity of each diskfile depends on the record length chosen and this is determined when the media is formatted.

Parameters germane to a format operation are as follows:

Bits per track	161,280
Overhead per record	1280 (bits)
Data field	Modulo 8 words

Table 1 shows typical record formats provided by the controller. The "record size code" is information used by the controller for read/write orders to determine the data field length.

TABLE I

Record Size Code	Data Words Per Record	Overhead Per Record (bits)	Total Bits Per Record	Records Per Track (dec.)	Record Addresses (decimal)	Wastage (bits) Per Track	Total Storage (Megabytes)	
							80 mb	300 mb
0	1040	1280	17,920	9	0-8	0	77	292
1	448	1280	8,448	19	0-18	768	70	266
2	512	1280	9,472	17	0-16	256	72	272
3	64	1280	2,304	70	0-69	0	37	140
4	128	1280	3,328	48	0-47	1,536	51	192
8	2048	1280	34,048	4	0-3	25,088	67	256

2.8 Record Addressing and Data Transfer Modes

A specific record is addressed by selecting one of four storage module devices, a specific cylinder using a seek order, a head and record using a read or write order. The controller contains data paths to transfer information to only one diskfile at a time. However, all diskfiles can seek simultaneously.

Data is transferred between the controller and memory using DMA. Data chaining operations (scatter/gather) are realized by use of multiple DMA channels. The software specifies the first channel number and the number of successive channels beyond one to be utilized. The controller will automatically switch to the next channel when the first one has reached end of range and continue until the last specified channel has been used. A maximum of 16 channels may be chained.

2.9 Record Read/Write

As detailed in paragraphs 2.5 and 2.7 above, each track is divided into records. The controller is informed, prior to execution of a data transfer instruction, the size of the data field to be expected. For a write order, the complete data field will always be written and the check field will always occupy the same physical location on the disk. Should DMA range and chain be exhausted prior to completion of writing a data field, the remaining portion of that field will be filled with undefined data.

2.10 Controller Data Buffering

The controller is provided with a 64 word RAM to buffer data between the disk and main memory. The RAM is organized as a FIFO (first in - first out) memory. Data is transferred between the FIFO and main memory in 8 word blocks such that CPU DMA latency need only be incurred once per 8 words transferred.

The serial bit rate of the storage module is 103 nano seconds per bit. This is equivalent to 1.65 u-seconds per word or 13 u-seconds per 8 word block. To a first approximation, the DMA must maintain an average level of service equal or better than this over the complete record in order that the FIFO should not overflow (read) or underflow (write). An individual block transfer time can be substantially greater than 13 u-seconds provided subsequent transfers allow "catch-up" to take place.

2.11 FIFO Operation for a Write Order

The FIFO is preloaded with 56 words of data during the search for the desired disk record. This preloading is done in 8 word blocks with a pause between blocks to allow lower priority controllers to use the I/O bus. The preloading has the effect of decreasing the level of service demanded from the DMA and the decrease is in proportion to the record length as shown in the following example.

Record length	1040 words
Preload	56 words
Balance to be transferred	984 words
Normal max block transfer	13 u-sec
Increased max block transfer	$\frac{13 \times 1040}{984}$ u-sec

If the FIFO is ever empty when a word must be sent to the disk, an underflow condition will occur and the DMX overrun status bit will be set.

2.12 FIFO Operation for a Read Order

If the average level of service of 13 u-seconds per block is maintained, the FIFO will have only one block left to transfer at the physical end of record. This will allow adjacent disk records to be read as explained in section 3.7. If the average level of DMA service is a little worse than 13 microseconds per block, then more than one block of data will remain in the FIFO at the physical end of record and the inter-record channel processing time available will be diminished. If a word is ever transferred from the disk to the FIFO when the FIFO is full, an overflow condition will occur and the DMX overrun status bit will be set.

2.13 Data Integrity

Four principal features contribute to data integrity of the storage module diskfile and its controller. These are as follows.

2.13.1 A 32 bit cyclic checkword follows each data record on the disk. This is a powerful check on the validity of the data from the controller/diskfile interface, to the magnetic media and back again. This is the same checkword scheme as used on controllers 4001/2/3 but the polynomial is changed such that error correction as well as detection is possible.

2.13.2 A 48 bit header, consisting of 32 information bits and 16 check bits, is recorded on the disk prior to each data field. The header provides a check that the desired record is actually being accessed. This, for instance, eliminates positioner errors from becoming a catastrophe (on write operations).

2.13.3 The controller is word-oriented with each data register, multiplexor and RAM carrying two byte-parity bits. For transfers of data to the diskfile, the actual byte parity from main memory runs right through the controller and is verified during formation of the cyclic checkword. For data transfers to main memory, byte parity is calculated prior to checkword validation; this parity is sent on the I/O bus to main memory and is checked by the CPU.

2.13.4 Diskfile selection, by a select order, is done in such a way that a positive response from the selected device is required. A check is also made that there is no duplicate selection. This feature will ensure that orders are being accepted by the desired storage module.

These four integrity features were not part of disk controllers 4001/2/3. Note that the controller parity feature (2.13.3) in inoperative with Prime 100 and other Prime CPU's not having parity generation and checking.

3.0 PROGRAMMING INFORMATION

3.1 General Description of Operation

The controller operates as a channel processor. This means that it receives its orders directly from a channel program located in main computer memory. The controller contains an order address register (OAR) whose function is analogous to

a C.P. program counter. The order address register is initially set to the starting location of the channel program by an OTA. Thereafter it is incremented following each channel program order (unless the order being executed is a jump to a new channel program address). The controller will continue executing channel program orders until a halt order is received. PIO instructions are minimized using this channel program technique.

3.2 Controller Bus Address and PIO Instructions

Model 4004 bus address is $(26)_8$ for the first controller and $(27)_8$ for the second. The following PIO instructions are available to this controller and are summarized in Table II.

PIO Commands - Model 4004 Controller

Op Code \ Function Code Bits 1-6 \ Bits 7-10	14_8 (OCP)	34_8 (SKS) (Skip If)	54_8 (INA)	74_8 (OTA)
00				
01				
02				
03				
04		Not Interrupting		
05				
06				
07				
10				
11			I.D.	
12				
13				
14				
15				
16	Clear Interrupt			
17	Initialize		Input OAR	Load OAR

TABLE II

3.2.1 OTA 17. Load Order Address Start

This instruction is used to load the order address register with a starting location for the channel program. The controller will only accept this instruction (cause a program skip) if it is non-busy.

After the controller accepts an OTA 17, it will become busy and A register bits 1 through 16 will be transferred to the controller's order address register. The latter points to a location in main memory which is the starting address of the channel program. With a 16 bit order address register, the disk channel program must be located within the first 64K of main memory.

The controller will fetch channel program orders one at a time using DMT. The orders will be executed as appropriate and the order address register will, in general, be incremented after each order to fetch the next one.

3.2.2 OCP 17. Initialize

This instruction will be accepted unconditionally by the controller. All control flip-flops will be reset and any operation in progress will be abandoned. The controller will be non-busy following execution of this instruction.

3.2.3 SKS 04. Skip if Not Interrupting

When the channel program order "interrupt" is executed, a controller interrupt flip-flop will be set. The state of this flip-flop is testable by this SKS instruction.

3.2.4 OCP 16. Clear Interrupt

The interrupt flip-flop referred to in paragraph 3.2.3 above will be cleared when OCP 16 is received.

3.2.5 INA 11. Input ID (Identification)

The controller ID may be read into the C.P.'s A register using this instruction. (The A register is not cleared before being loaded by this instruction.) This instruction is only accepted by the controller when the controller is non-busy and can therefore act as a busy test. The ID format is standard with slot number in bits 4-8 and device address in bits 11-16. Other bits are zeros.

3.2.6 INA 17. Input Order Address Register

The contents of the Order Address Register (OAR) may be read into the CP's A register using this instruction. As the OAR is not cleared by OCP Initialize or Master Clear, this INA can be useful for system maintenance following a malfunction. INA 17 is accepted by the controller only when it is non-busy and can therefore act as a busy test. Note that the A register is not cleared before being loaded by this instruction.

3.3 Channel Orders

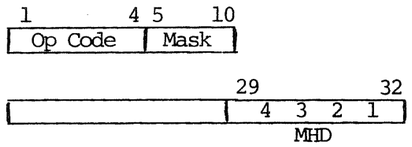
Fourteen channel program orders are available to the controller. Each order has a four-bit op code located in bits 1 to 4. All but three orders are two words long. Bits in the first word are numbered from 1 to 16 and in the second word from 17 to 32. Bits in the third word (where applicable) are numbered from 33 to 48. Unused bits should be set to zeros to allow future product expansion without generating possible program difficulties.

3.3.1 Conditional Execution of Orders

Each order has a six-bit mask field in bits 5 to 10. Each of mask bits 6 to 10 relate to a specific controller or device condition. When a particular mask bit is set, the related controller (device) condition is tested and execution of the instruction is dependent on the result of the test. If all mask bits are set to zero, the instruction is unconditionally executed. Mask bit 5 is used to reverse the result of the test. Specific definition of the mask field is given in paragraph 3.5 below.

3.3.2 Select Order

This order is used to condition the controller to address one of the four possible devices. Format of the instruction is as follows:

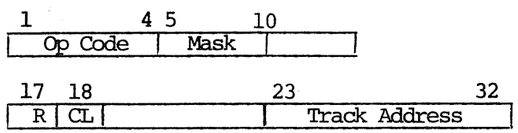


Op Code - 4 (hex)
Mask - defined in paragraph 3.5
Bits 29-32 - Select one of four MHD's by setting one of these four bits. If this field is zero, the previously selected MHD will be de-selected.

Once a specific device is addressed using this order, it will remain addressed until another select order is given or the controller is initialized. For dual-port operation, de-selecting a device will make it available to the "other" controller.

3.3.3 Seek Order

The primary purpose of this order is to cause the head positioner of a previously selected MHD to move to a specified track. A secondary function is to act as a programmed initialize (fault clear) to the selected diskfile. Format of the order is as follows:

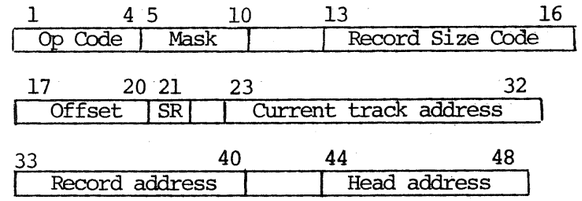


Op Code - 3 (Hex)
Mask - defined in paragraph 3.5
Bit 17 - If set, the head positioner will do a slow seek to track zero. The track address field is ignored.
Bit 18 - If set, the selected diskfile will be cleared of any faults provided that the situation which caused the fault has been rectified.
Bits 23-32 - Used to select one of 823 tracks. Valid addresses go from $(000)_8$ to $(1466)_8$.

3.3.4 Read Record/Write Record

These two orders address a specific head and record on a previously selected diskfile and read data from or write data into that record. Either of these orders

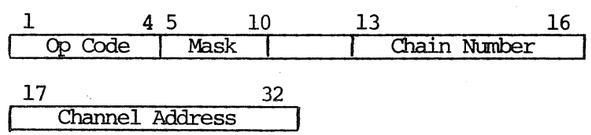
may be given while the selected diskfile is seeking. Execution will stall until the head positioner has finished moving. Order format is as follows:



Op Code - 5 (Hex) read record
- 6 (Hex) write record
Mask - Defined in paragraph 3.5
Record size code - This code is taken from Table I and informs the controller how long is the data field of the desired record.
Offset - This field is normally zero. It is used for error recovery. See paragraph 3.9.
SR (short read) - This bit is normally zero. It is used to assist disk latency optimization. See paragraph 3.6.
Current track address - This field is to be set to the track address of the last seek order to the selected diskfile.
Record address - An eight bit field which defines one of n records on the selected track. Record addresses are sequential from zero to the maximum value which can be determined from Table I.
Head address - A five bit field which defines one of 19 heads for 300 megabyte files and one of 5 heads for 80 megabyte files.

3.3.5 Channel Address

This order informs the controller which DMA channel and how many channels are to be chained for data transfers. Order format is as follows:



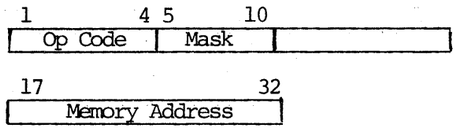
Op Code - D(Hex)
Mask - Defined in paragraph 3.5
Chain number - The number of successive DMA channels beyond one to be used for data transfer.
Channel address - A field which informs the controller which DMA channel to use at the beginning of data transfers.

This order will normally be given prior to a read or write record order. The channel address is stored in the controller in a register which is also used by the following channel program order: Input Status, Input OAR, Interrupt, Load and Store.

Execution of these orders following a channel address order will cause the channel address to be lost.

3.3.6 Input OAR

The contents of the order address register will be read into memory when this order is executed. Format of the order is as follows:

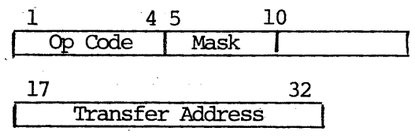


Op Code - B (Hex)
Mask - Defined in paragraph 3.5
Bits 17-32 - A 16 bit memory address which defines the location into which the OAR is to be read.

The OAR is incremented following the fetch cycle of each channel order. Therefore, if an input OAR channel order is in location X in memory, a value of X + 2 will be transferred to the location specified by bits 17-32.

3.3.7 Transfer Channel Program Address

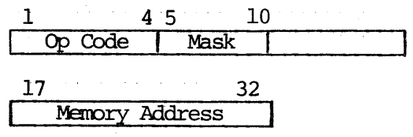
Execution of this order will cause the controller's order address register (OAR) to be loaded with a new value. This order is analogous to a CPU jump except the transfer can be made conditional using the mask field. Order format is as follows:



Op Code - F (Hex)
Mask - Defined in paragraph 3.5
Bits 17-32 - The new value to be loaded into the OAR.

3.3.8 Input Status

Controller status, defined in paragraph 3.4 below, may be input to memory using this order. Format of the order is as follows:



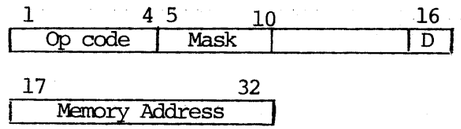
Op Code - 9 (Hex)
Mask - Defined in paragraph 3.5
Bits 17-32 - A 16 bit memory address into which the status information is to be transferred.

3.3.9 Load and Store

A word of data from high-speed memory will be sent to the controller on execution of the load order. The same data word will be sent to high-speed memory on execution of a store order.

Information from these two orders is held within the controller in one location in the FIFO memory.

Format of the two orders is as follows:



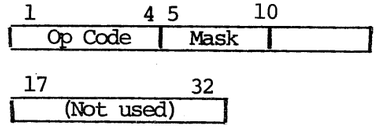
Op Code - A (Hex) Store
C (Hex) Load
Mask - Defined in paragraph 3.5
Bit 16 - Normally set to zero. Used for diagnostic testing of the FIFO as explained below.
Bits 17-32 - A 16 bit memory address whose contents are loaded into the controller or into which data from the controller is stored.

The data output from memory is stored in the controller in a register shared by other instructions. A read record or write record instruction will cause the data sent by a previous load instruction to be lost.

As mentioned above, load and store data is held in the controller in the FIFO memory. If bit 16 of the order is set, the FIFO address counters are not cleared prior to execution of the order but are incremented following execution. In this way successive FIFO locations can be filled using load orders or emptied using store orders.

3.3.10 Halt

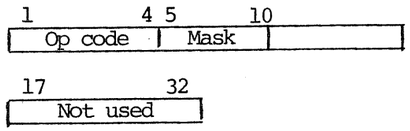
Execution of this order will cause the channel program to come to a stop and the controller to go non-busy. This means that an OTA 17 can be accepted and, in fact, this is how the channel program is restarted. Format of the halt order is as follows:



Op code - 0 (Hex)
Mask - Defined in paragraph 3.5
Bits 17-32 - The second word of the instruction is unused.

3.3.11 Stall

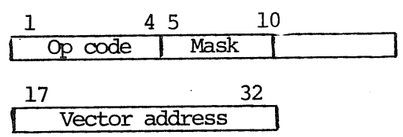
This order is equivalent to a NOP instruction which takes 210 microseconds to execute. Its purpose is as follows. Certain channel program loops may depend on a mechanical event to allow an exit from the loop (e.g., the head positioner reaches the desired track). Continuous execution of the orders in the loop would consume a lot of computer time without achieving any meaningful results until the desired event takes place. The addition of a stall order to the loop would mean the desired event is only tested about every 210 microseconds. However, the central processor can be doing meaningful tasks between tests (i.e., during execution of the actual stall order). The format of this order is as follows:



Op code	- 7 (Hex)
Mask	- Defined in paragraph 3.5
Bits 17-32	- The second word of the instruction is unused.

3.3.12 Interrupt

The controller will cause an I/O bus interrupt to take place when this order is executed. The controller will suspend processing further channel orders until an OCP 16 (clear interrupt) is issued. Format of the order is as follows:



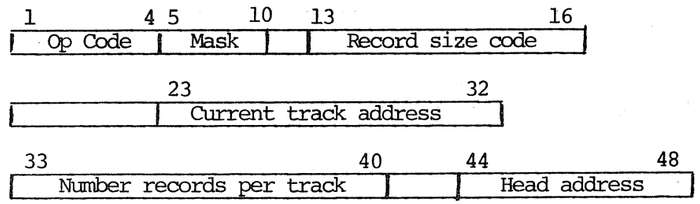
Op code	- E (Hex)
Mask	- Defined in paragraph 3.5
Bits 17-32	- A 16 bit vector address placed on the I/O address bus for the duration of the interrupt.

The vector address field must be specified when the central processor is working in the vectored interrupt mode. There is no default vector address value.

When the interrupt order is executed, a controller flip-flop is set and this causes SKS 04 to not skip. The flip-flop is cleared by OCP 16 and controller channel processing will resume.

3.3.13 Format

This channel order is used to write headers on a virgin disk or to rewrite headers on a disk whose format is to be changed. Execution of this order will cause n headers to be written on the selected diskfile at the current track. The head to be used and the value of n are defined by fields in the order. This is a 3 word channel order whose fields are similar to those of a write.



Op code	- 2 (Hex)
Mask	- Defined in paragraph 3.5
Record size code	- Taken from Table I. Defines to the controller the length of the data field of each record on the track.
Current track address	- This field is to be set to the track address of the last seek order to the selected diskfile.
Number of records per track	- This information is taken from Table 1 and allows the controller to know when the track has been formatted.
Head address	- A five bit field which defines one of 19 heads for 300 megabyte diskfiles and one of 5 heads for 80 megabyte diskfiles.

Each format order writes a complete track with each record being recorded as detailed in paragraph 2.5 above. The data field will be "ones" and a valid checkword is written. Each record on the track is of equal length with sequential record addresses. Record address zero follows the "Index" pulse - a once-per-revolution timing signal supplied by the storage module diskfile.

Two revolutions of the diskpack plus a wait-for-index are required to format each track. The first revolution writes "zeros" round the complete track to ensure that no false address marks are detected on a subsequent read order.

3.3.14 Undefined Channel Orders

There are two undefined channel orders whose op codes are 1 and 8 (Hex). Attempted execution of these orders will cause the channel program to halt, but the controller will remain busy. This condition will have to be cleared by OCP 17.

3.4 Status Word

The status word may be input to memory as explained in section 3.3.8 above. Bits of the word are defined as follows:

- Bit 1 - Unconditionally a logic 1 to act as a flag bit.
- Bit 2 - DMA overrun. Set if the CPU failed to respond to transfer requests from the controller within the allotted time (defined in paragraphs 2.10/11/12).
- Bit 4 - Check error. Set if during a read operation the data read and the check field do not balance.
- Bit 5 - Controller data parity error. A transient (or permanent) error has been detected during a write or format order.
- Bit 6 - Header check failure. Set when the previous read/write order failed to match the header from the disk against the desired header.

Bit 11 - For dual port devices only. Set when the selected device is busy servicing a controller on the other port.
Bit 12 - A "zero" but reserved for write-protect status if this feature is made available in the future on storage module diskfiles.
Bit 13 - Set when the selected diskfile is seeking.
Bit 14 - Illegal seek. Set under three circumstances: (a) the head positioner was unable to complete a seek within a specific time period; (b) the carriage has moved to a position outside the recording field; (c) an illegal track address was received by the selected diskfile.
Bit 15 - Select error. A select channel order resulted in a duplicate or illegal device selection. Manual intervention may be needed.
Bit 16 - Unavailable. The selected diskfile is not ready for use and manual intervention may be needed.

The illegal seek status bit (bit 14) can only be cleared by issuing a restore to track zero to the offending diskfile.

Status bits 2,4,5 and 6 will be cleared by execution of a read or write record or format channel order. They are not cleared by OCP initialize so that the conditions may be preserved in the event of a controller "lock-up".

The conditions that caused status bits 2,4 or 6 to be set during a write record operation will cause a zero check word to be written on the disk for that record. This will guarantee a check error when the record is subsequently read.

A select error (status bit 15) will be cleared by another select channel order provided the condition that originally caused the error has been rectified.

A header check failure (status bit 6) implies either or both of these situations:

(a) A match between the wanted header and headers from the disk could not be made within 128 attempts;

(b) A match was made but the header checkword would not balance. In either of these situations, the read/write order is completed in the sense that data transfers take place to/from memory. No data is written on the disk of course.

CHANNEL ORDER SUMMARY - MODEL 4004

Order	Op Code	Mnemonic	Execution Time (u-s)	Fields	
Halt	0	DHLT	6		
Format	2	SFORM		Rec Size	13-16
				Track Addr	23-32
				# Records	33-40
				Head Addr	44-48
Seek	3	SSEEK	7.5	Restore	17
				Clear	18
				Track Addr	23-32
Select	4	DSEL	7.5	MHD	29-32
Read	5	SREAD		Rec Size	13-16
				Offset	17-20
				SR	21
				Track Addr	23-32
				Rec Addr	33-40
				Head Addr	44-48
Write	6	SWRITE		Rec Size	13-16
				Track Addr	23-32
				Rec Addr	33-40
				Head Addr	44-48
Stall	7	DSTALL	210		
Input Status	9	DSTAT	9	Mem Addr	17-32
Store	A	SSTOR	9	Diag Addr	16
				Mem Addr	17-32
Input OAR	B	DOAR	9	Mem Addr	17-32
Load	C	SLOAD	9	Diag Addr	16
				Mem Addr	17-32
Channel Address	D	SDMA	6	Chain	13-16
				Chan Addr	17-32
Interrupt	E	DINT	6+CPU	Vect Addr	17-32
Transfer	F	DTRAN	6	Trans Addr	17-32

NOTE: All orders have op code in bits 1-4 and mask in bits 5-10.

TABLE III

3.5 Instruction Mask Field

As mentioned in paragraph 3.3.1 above, the execution of each channel instruction can be made to be conditional on certain controller or device conditions by use of the six bit mask field in each instruction word. The following table shows the effect of setting mask bits 6-10 with mask bit 5 cleared and set.

Bit 5 = 0, do not execute instruction if:

Bit 5 = 1, execute instruction if:

Set Bit	
6	No function but reserved for "selected diskfile is write protected."
7	Last read or write record instruction caused a DMA overrun, check error, controller parity error or header check failure (status word bits 2,4,5 or 6 set).
8	Selected MHD is seeking.
9	Selected diskfile has an error condition (status word bits 14, 15 or 16 are set).
10	For dual port operation only. Selected diskfile is busy servicing the "other" controller.

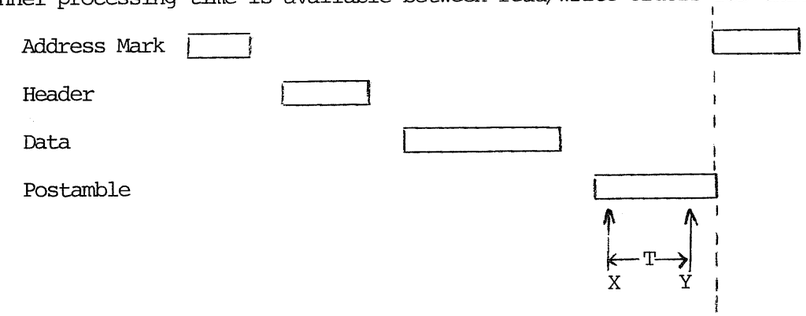
Two or more conditions may be tested simultaneously and will give a logical OR of the individual conditions.

3.6 Latency Optimization

Disk latency can be optimized by use of the short-read feature mentioned in 3.3.4. This feature causes a read order to read the next available record on the disk and to terminate at the end of range and chain (as opposed to after the check word has been read and verified). For instance, if the record address has been written in the first word of each data field, then a short-read order can be used to input the next available record address to main memory. Future decisions can be made based on the received record address while the controller will be executing further channel orders.

3.7 Inter-record Channel Processing Time

It may be desirable to read/write sequential records round the disk surface. Channel processing time is available between read/write orders for this purpose.



The above figure shows the format of a typical record. A read/write order will end at point X. Next read/write order must start by point Y to catch the next record. Time T is the time available for executing orders between two read or write orders. For a write order, point X occurs after 8 bits of postamble and T is equal to 58 u-seconds. For a read order, point X occurs when the FIFO memory is empty and T will usually be at least 49 u-seconds. Point Y is fixed relative to the next record for both a read or a write of that record.

The inter-record channel processing time T is used as follows. Suppose a sequence of channel orders to read two adjacent disk records is

Read record N	
Input status	9 u-seconds
Transfer	6 u-seconds
Setup DMA channel	6 u-seconds
Read record N+1	

The total execution time of the three channel orders between the two read orders is 21 u-seconds. As this is less than T (equal to 49 u-seconds), record N+1 will be read without an extra disk revolution.

3.8 Check Word and Error Correction

Each record written on the disk is followed by a 32 bit checkword. The checkword is calculated by dividing the data in the record (the message) by a certain polynomial. This yields a quotient which is discarded and a remainder which is defined to be the checkword.

On reading a record, the message and checkword are divided by the polynomial. The remainder from that division will be zero if no errors occurred in the message or checkword. If errors did occur and the message cannot be recovered by traditional means, error correction can be attempted. This is explained in Appendix A and is a software technique. It involves reading the record and checkword into memory.

This may be done as follows. Suppose the media has been formatted to give 9 records per track. As shown in Table I, each record will have 1040 data words for a record size code of 0. A read order with a record size code of 8 will tell the controller that the data field is 2048 words long and the controller will transfer this number of words to memory provided sufficient DMA range is provided. Words 1041 and 1042 will be the check word. One should expect a check word error to set in the status field.

3.9 Error Recovery Procedures

Storage module diskfiles are provided with two features to assist in reading a record that appears to be irrecoverable. They are as follows: (a) the heads may be positioned off-track in either direction; this is called servo+ and servo-; and (b) the read data may be sampled early or late with respect to the nominal sample; this is called strobe+ and strobe-.

The read record channel order has an offset field, bits 17-20. This field controls the servo and read circuitry in accordance with the following table.

Set to 1	Action	
Bit 17	Servo+	Move heads in
Bit 18	Servo-	Move heads out
Bit 19	Strobe+	Strobe data early
Bit 20	Strobe-	Strobe data late

Eight legal combinations are possible for error recovery and the potentially irrecoverable record should be read several times with each before being abandoned.

The offset field has no effect on write or format orders.

3.10 Power Up/Down

Normal system procedure would be to stop all storage module diskpacks before removing power from the controller. The controller is provided with a power fail relay and this will inhibit any writing on the disks if controller power goes down before storage module power. On restoring controller power it may be necessary to issue a restore to zero to all storage module diskfiles to clear a phoney illegal seek situation (status bit 14 set).

APPENDIX A

Error Correction of Data Records

A.1 Introduction

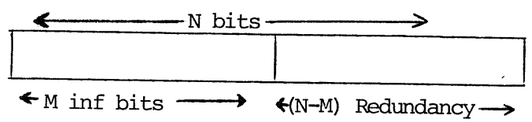
Storage Module media is not as perfect as CDC would like it to be. The bit recording density of about 6000 bpi is state of the art and requires a head flying height and coating thickness of about 20 micro-inches. (The figure for 2314 type packs is 60 micro-inches.)

Practical testing has revealed that 100% of all unrecoverable errors are one, two or three bit bursts. CDC specify that a track shall not have more than one burst error and it, in turn, shall be no longer than 11 bits long. Cylinder 0 (heads 0 and 1) shall have no errors. Also, there shall be no more than 30 correctable error tracks per pack.

Based on the above, a viable Storage Module system must have the ability to either bypass bad tracks or to perform error correction on them. The former technique relies on the fact that the pack vendor must be able to tell the customer the locations of all the bad tracks. As CDC are unable, by their own admission, to do this, the only practical solution to the problem is an error correction scheme.

A.2 Principles of Error Detection

As explained in paragraph 3.8 above, a checkword is appended to the message (data field) when the information is written on the disk. The checkword is obtained as the remainder when the message is divided by a carefully chosen number known as the generator polynomical.



The above figure shows a message of M information bits having added to it (N-M) redundancy bits. The redundancy bits are achieved as follows:

Let M(X) equal the message polynomial.
Let P(X) equal the generator polynomial.

Hence $M(X) = Q(X)\ P(X) + R(X)$ where Q(X) and R(X) are respectively the quotient and remainder following division. The quotient has no real significance and is discarded but R(X) becomes the (N-M) redundancy bits shown above. Hence the total message (information plus redundancy) can be expressed as:

$$N(X) = X^{(N-M)}\ M(X) + R(X)$$
$$= Q(X)\ P(X)$$

If the received message can be divided by the polynomial P(X) without a remainder, then it has been received correctly and further action is not needed.

A.3 Choice of Polynomial

The strength or weakness of a redundancy scheme is intimately tied to the choice of polynomial and this depends on the type of errors to be expected. Data transmission suffers from long burst errors. High-speed solid-state memories suffer from isolated single-bit errors. Rotating magnetic memories compromise between these two extremes and suffer from short bursts (1-3 bits). The polynomial chosen was a Fire code and thus is of the following form:

$$P(X) = Pl(X)\ (X^C+1)$$

where P(X) is the generator polynomial for a Fire code; this must have two properties. (1) Pl(X) is a primitive (irreducible) polynomial of degree M and order E. (Note, the degree of a polynomial is defined to be the greatest power of X in which the coefficient is non-zero and E is defined to be (2^M-1).) (2) The parameter C must not be divisable by E.

The above Fire code polynomial will have the following properties: (1) The length of the code, N, is equal to the least common muliple of E and C. This works out to be $(2^M-1)C$. (2) The number of redundancy bits is equal to (M+C). (3) The number of information bits, M, is equal to $(2^M-1)C-(M+C)$.

The polynomial chosen for the Storage Module Controller is as follows:

$$P(X) = (X^{11}+X^2+1)(X^{21}+1)$$

The degree of the Pl(X) portion is 11 and E is therefore equal to $(2^{11}-1)$ or 2047. The length of the code is equal to (E·C) where C equals 21. Hence, code length equals (2047·21) bits. The number of redundancy bits is equal to (M+C) or (11+21).

In summary, the above polynomial will support a record length up to 2680 words and each record will be followed by a 32 bit checkword.

A.4 Error Detection and Correction Performance

The polynomial chosen was $P(X) = (X^{11}+X^2+1)(X^{21}+1)$

$$= X^{32}+X^{23}+X^{21}+X^{11}+X^2+1$$

This will detect two error bursts of combined length 22, one error burst of length 32 and any odd number of errors. This will correct any single burst up to 11 bits long.

A.5 Practical Details

The controller generates the 32 bit checkword as per P(X) above when writing data on the disk. The controller also performs all error detection on reading records. The burden of error correction is placed on system software and the method of performing correction is as follows:

1. Read record and 32 bit checkword into memory (as per paragraph 3.8).
2. Pass record and checkword through a 32 bit software check register (SCR). This register duplicates the hardware check register in the controller and divides the record and checkword by the generator polynomial P(X).
3. The chosen polynomial has a natural message length of $(2^M-1)\cdot C$ or 42987 bits. Zero bits must be passed through the SCR as if the message has this total number of bits.
4. The correction phase can now begin. The SCR can be thought of as split into two sections.

1 — 21	22 — 32
test for all zeros 21 bits	correction pattern 11 bits

When SCR bits 1-21 are zeros, bits 22-32 will contain a correction pattern that can be applied to the data from the disk. The method is to cycle the SCR one bit at a time (with zero data input) until SCR bits 1-21 are zero. The data read from the disk is also conceptually cycled in a buffer one bit at a time. When SCR bits 1-21 are zero, SCR bits 22-32 contain a correction pattern and this is exclusive-ored with the next 11 read data bits to perform the actual error correction.

If SCR bits (1-21) are never zero within 42987 shifts, the error is uncorrectable.

A.6 More Sophisticated Error Correction

The method of performing error correction as described in paragraph A.5 is quite logical, but very slow in terms of CPU instructions executed. PRIMOS achieves a 15:1 improvement over the method detailed in paragraph A.5 (which is the method used by test program DISCT2). In practical terms, this reduces a typical error correction from 1·2 seconds to 80 milliseconds for a PRIME 300.

FEtch + Setup PAGE 1 OF 2

FEtch 1 +
FEtch 2 +
FEtch 3 +
pause +
Setup +
CLpHR −
CNDRQ +
FEADP +
myDst +
DmtBy +
StBDy +
F3YES +
OP code AND EX VALid
FEtip +
DENAL +
FNSC8 +
Bit CntR VAL
BPCFC +
OSCEN +
BCCLK +
SELtAG +
HDtEN +
TAGEN +
VALid HEAD/tRACk INF to Smcl
ContAG +
SEttp +
SDMtR +
IORHS +
FLLLF +
F Busy +
TREGCk +

NOT EX, TRANS, DMxAD

SEEK OR SELECT

READ, WRITE, Format ONLY

ALL other ORDERS

LOAD I/P OAR/STAT, WRITE

StORE

SA/HA to HEADER REG DMtBY +

SET FOR FEtch BUT DON't CARE

TRACk to HEADER REG Load OFFSET REG

READ/write FORMAT ONLY

Setup REC Size Chain Etc IF EXECUTE

STEP DRC TO 1

STEP DRC TO 2

DENAL GOES High FOR Load/ StORE I/P OAR/STAT

DENAL+

StBDY+

StORE/IP STAT ETC

ASSUME DENAL GOES LOW AFTER myDSt+

DPCC8+

DIFFERENT TIMMING FOR LOAD ORDER

X | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

CLR IF (SEL ∧ EX)

HEAD OR CYL TAG AS APPROPRIATE

SAMPLE FOR DUP SELN FOR SELECT ORDER

SETUP ∧ EX

WRITE REG → ABMC
WRT REG → FIFO
OAR (+TRANSFER)
READ REG

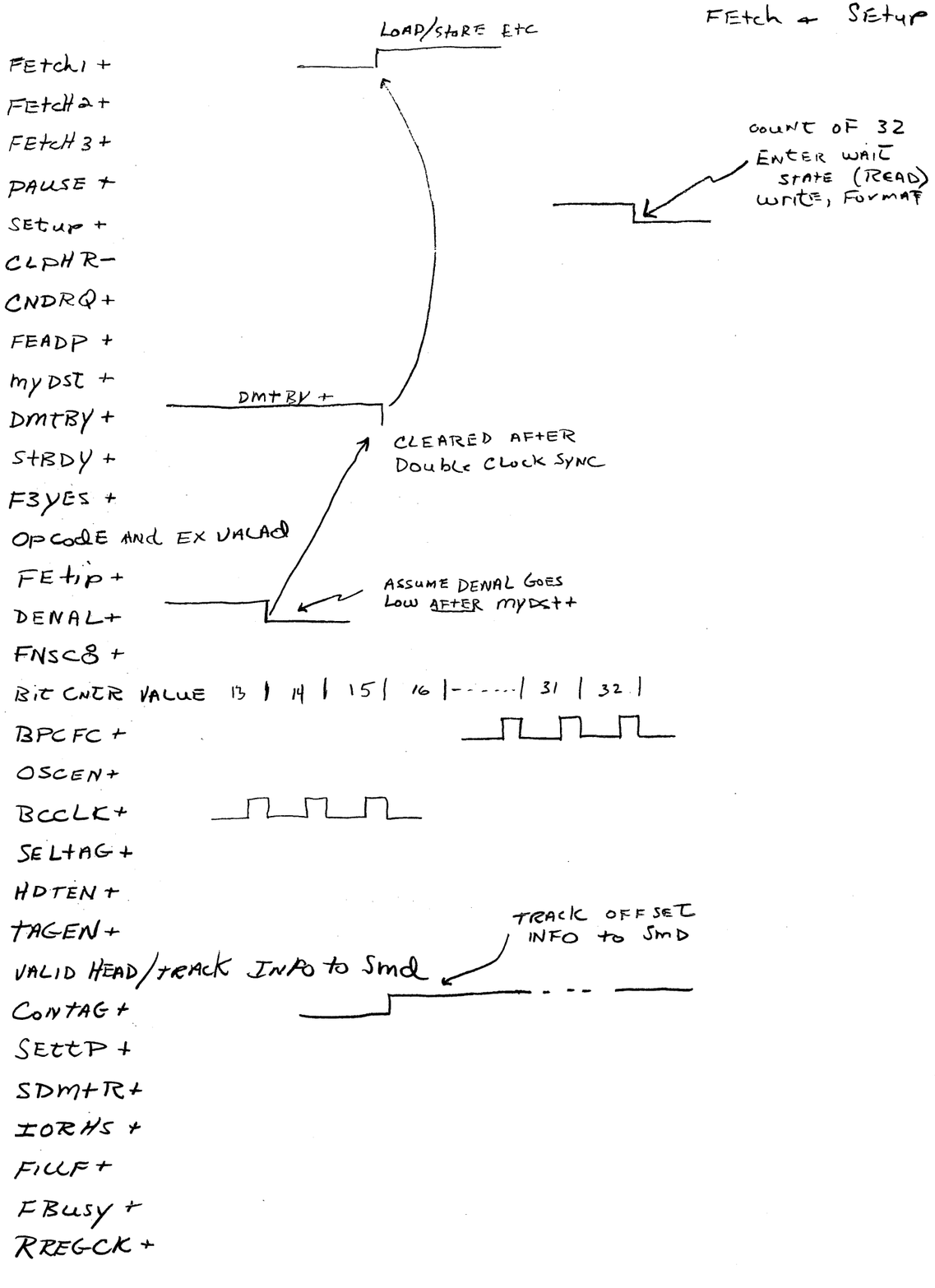
StORE ONLY

FOR FORMAT LOAD TRKC

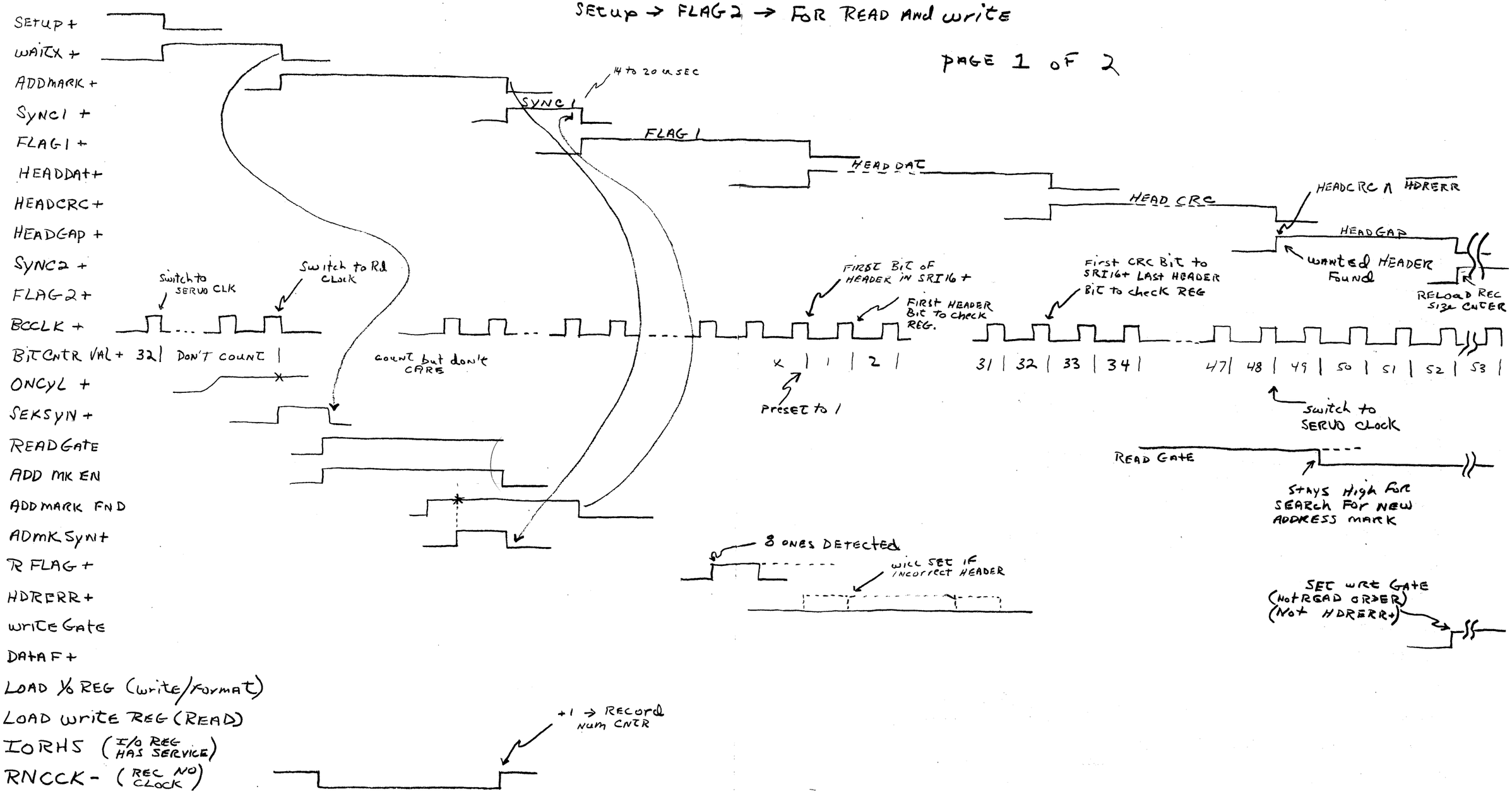
LOAD ORDER WRITE REG to FIFO

I-14

PAGE 1 OF 2


LOAD/STORE ETC
FEtch1 +
FEtch2 +
FEtch3 +
PAUSE +
SEtup +
CLPHR-
CNDRQ +
FEADP +
myDST +
DMTBY +
STBDY +
F3YES +
OPCODE AND EX VALAD
FETip +
DENAL+
FNSC8 +
BIT CNTR VALUE 13 | 14 | 15 | 16 |------| 31 | 32 |
BPCFC +
OSCEN+
BCCLK+
SELTAG +
HDTEN +
TAGEN +
VALID HEAD/TRACK INFO to Smd
CONTAG +
SETTP +
SDMTR+
IORHS +
FILLF +
FBUSY +
RREGCK +
COUNT OF 32
ENTER WAIT STATE (READ) WRITE, FORMAT
DMTBY +
CLEARED AFTER Double Clock SYNC
ASSUME DENAL GOES LOW AFTER myDst+
TRACK OFFSET INFO to SmD

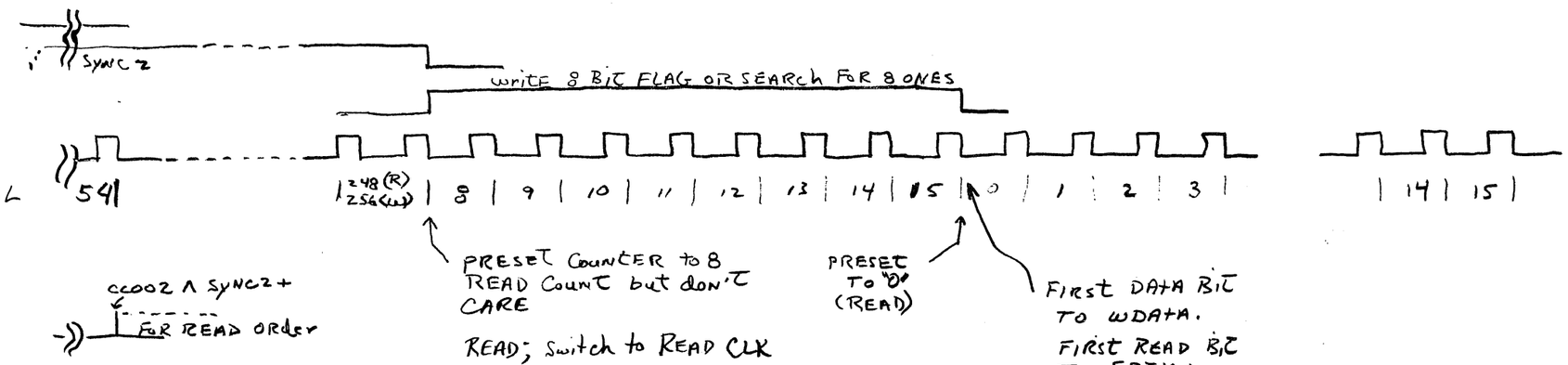
Setup → FLAG 2 → For Read and write



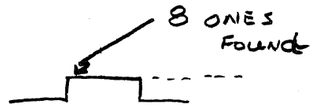
I-16

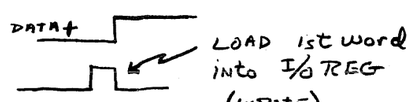
SETup → FLAG2 → For READ and write

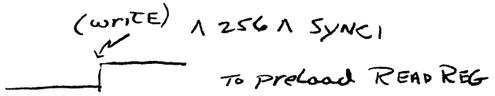
SetUp +
WAITx +
ADDMARK +
SYNC1 +
FLAG1 +
HEADDAT +
HEADCRC +
HEADGAP +
SYNC2 +
FLAG2 +
BCCLK +
BIT CNTR VAL
ONCYL +
SEK SYN +
READ GATE
ADDR MK EN

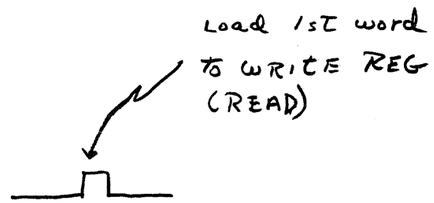


ADDR MK Found
ADMK SYN+
RFLAG+
HDTRERR+
WRITE GATE
DATAF +
LOAD I/O REG (write/Format)
LOAD write REG (READ)
IOTRHS + (I/O REG HAS SERVICE)
RNCCK (REC NO clock)

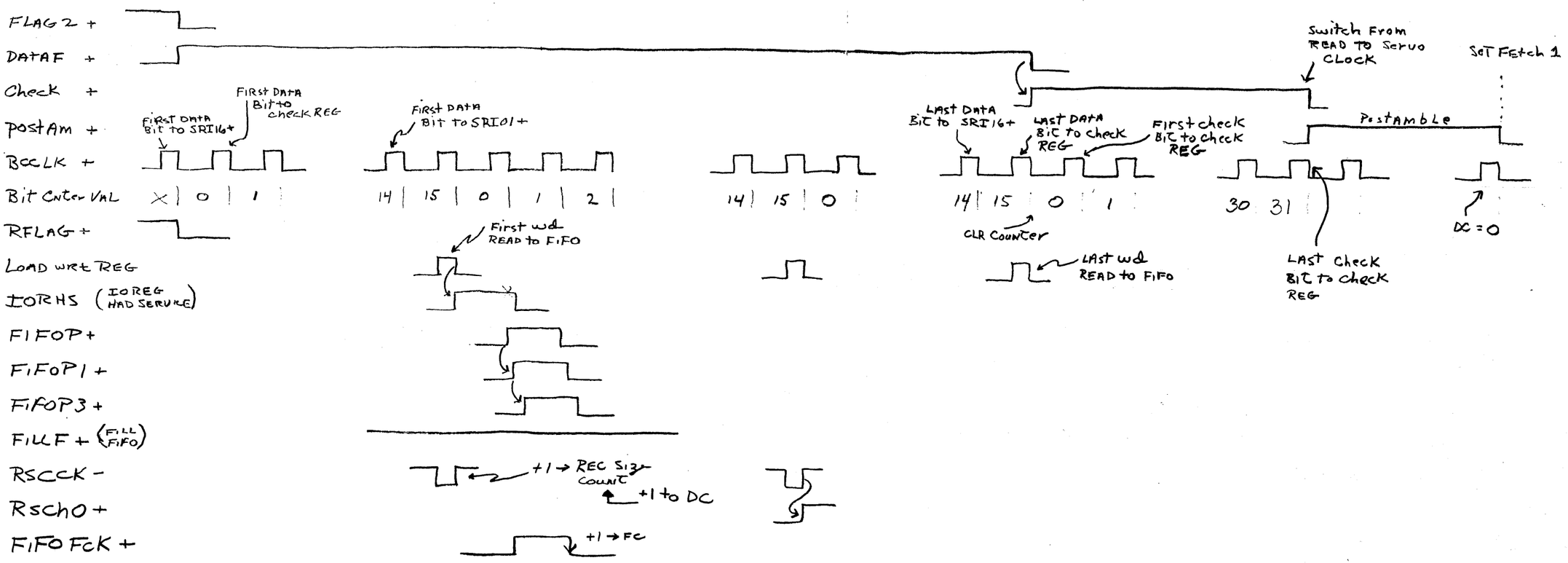




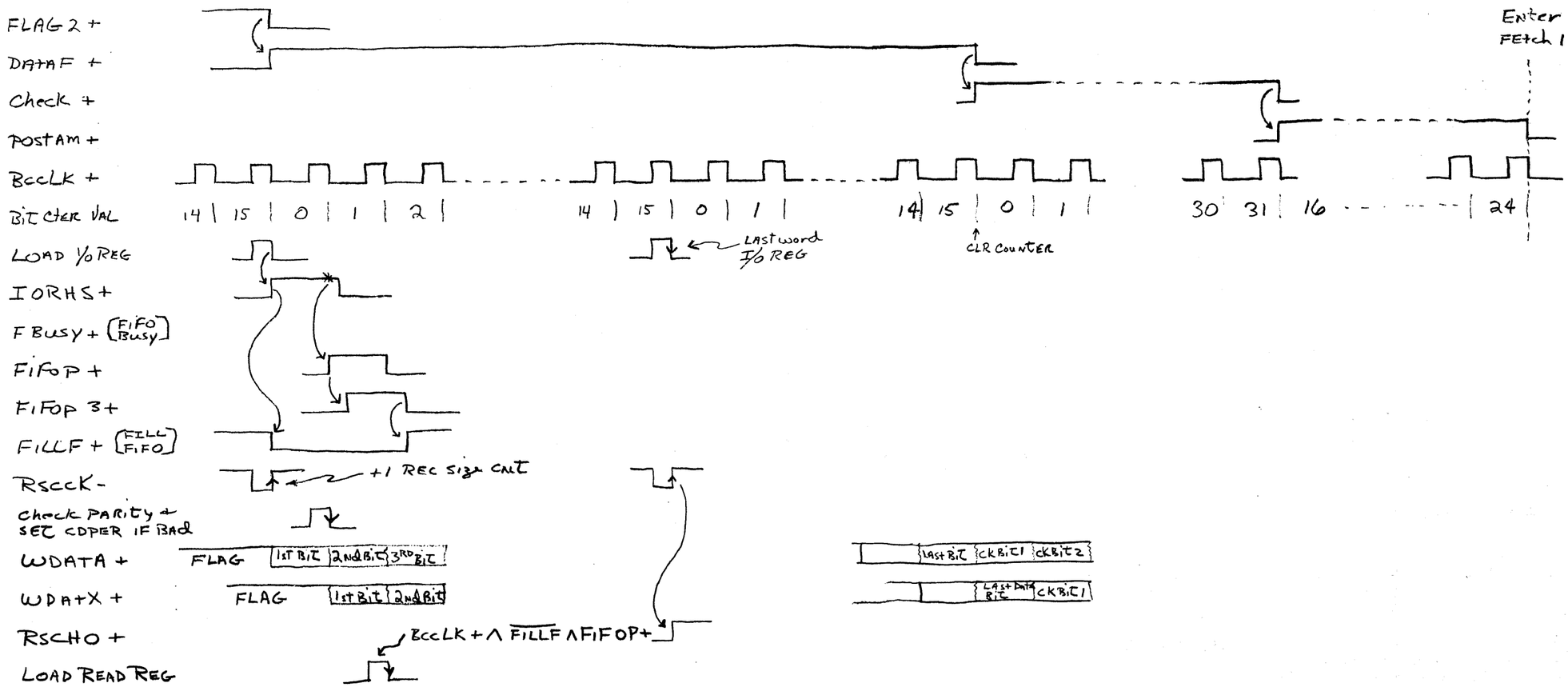




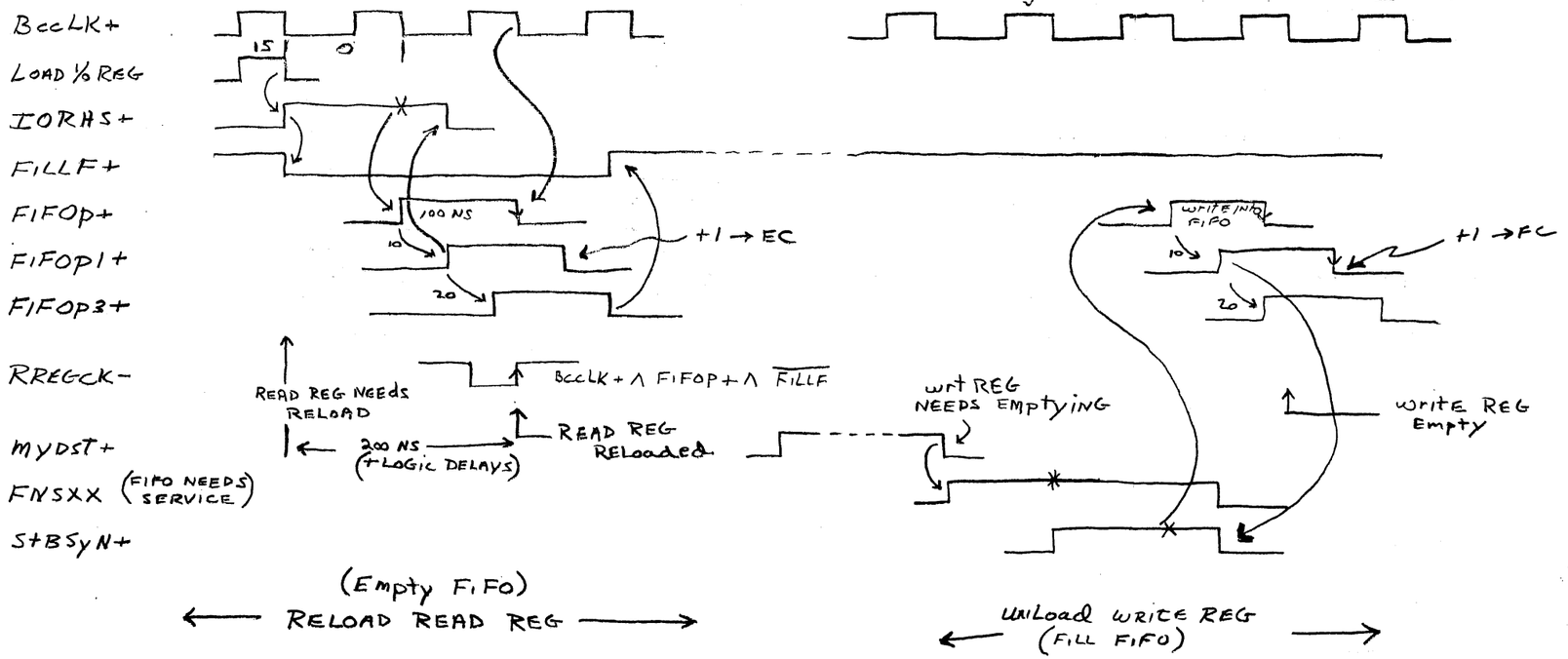
READ ORDER; FLAG 2 → Fetch 1 [smc]



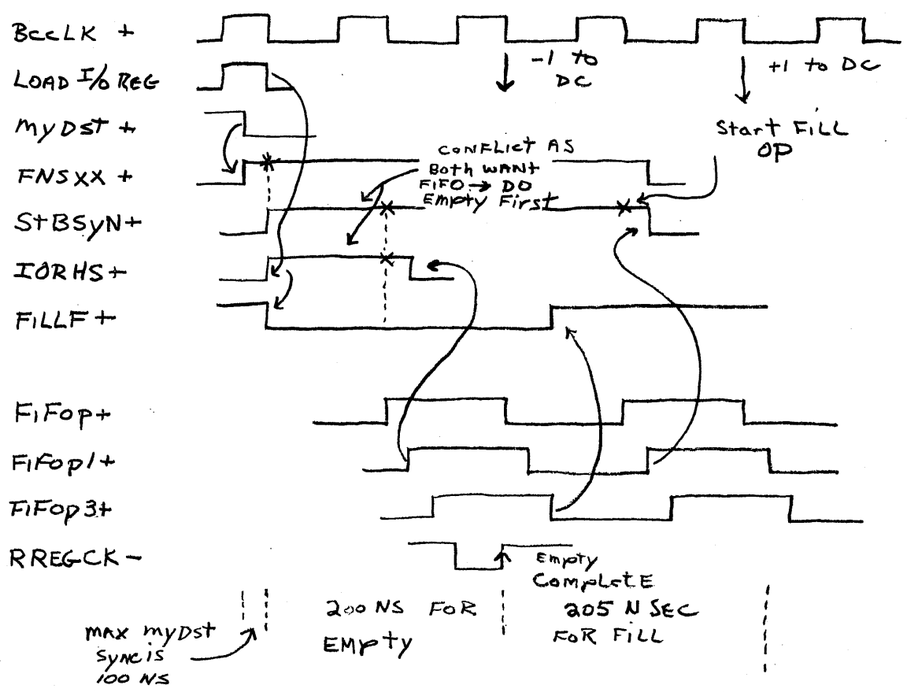
WRITE ORDER : FLAG 2 → Fetch 1 [SMC]



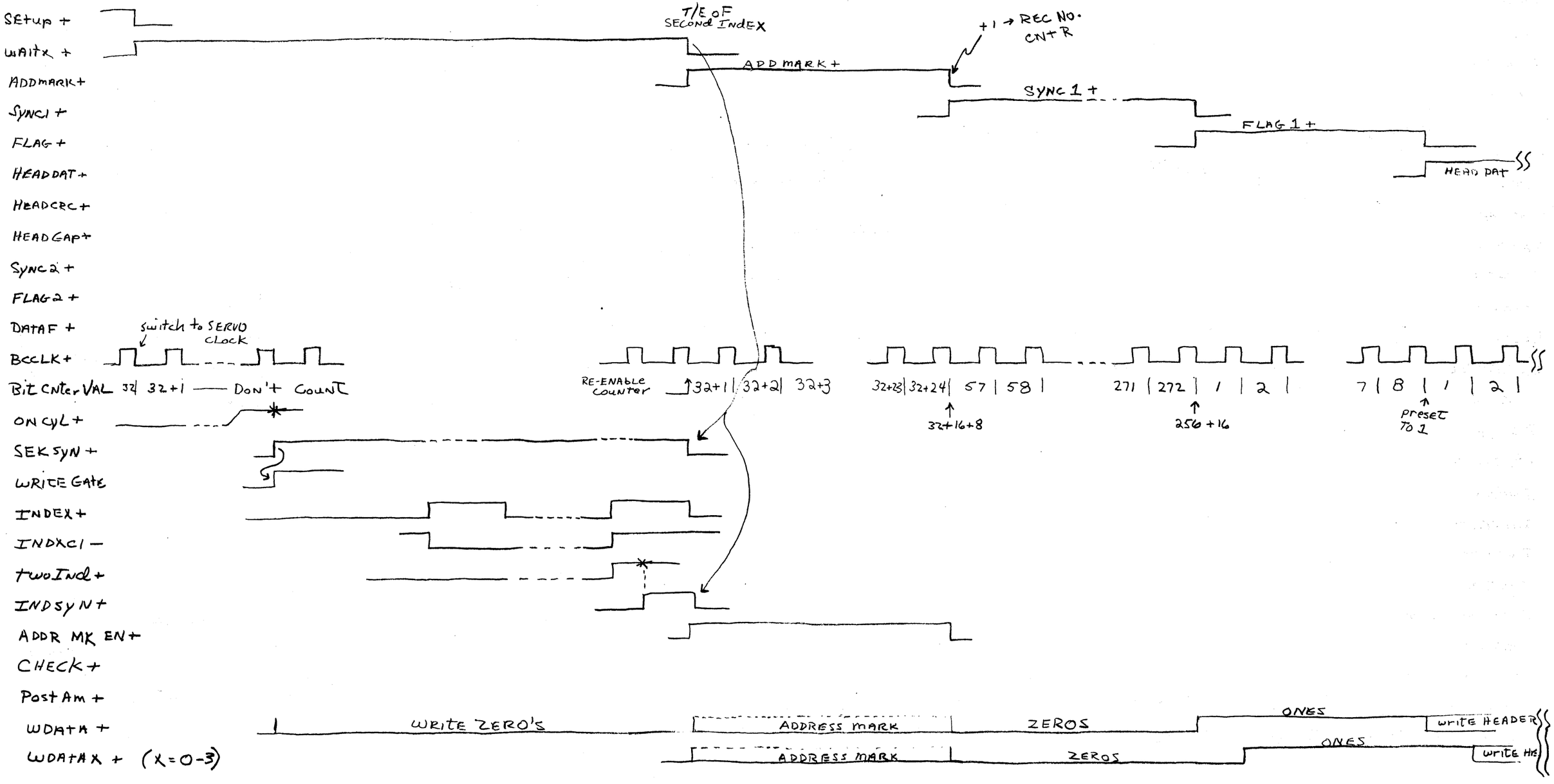
FIFO Timing [Write to Disk [SMC]]

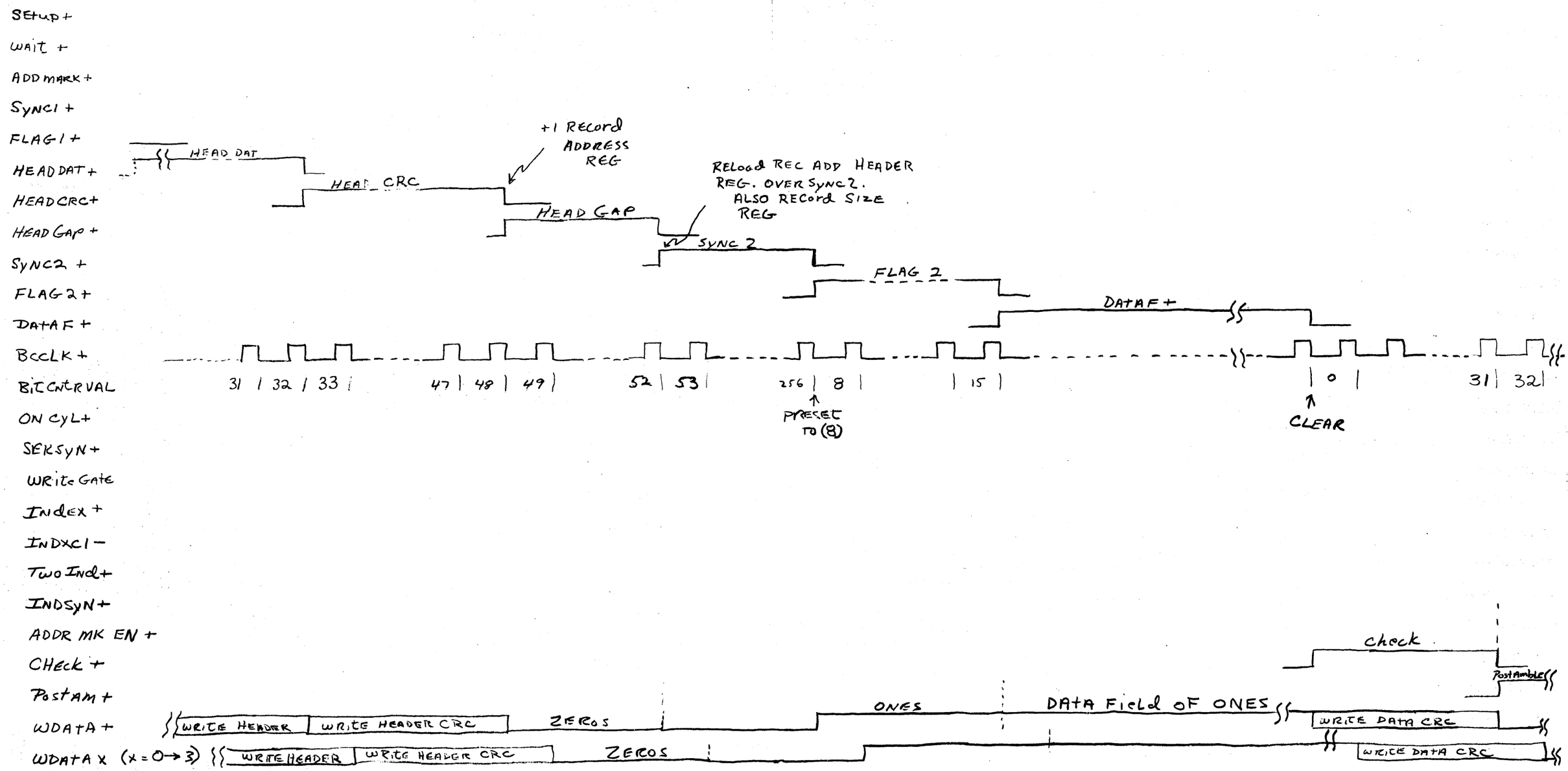


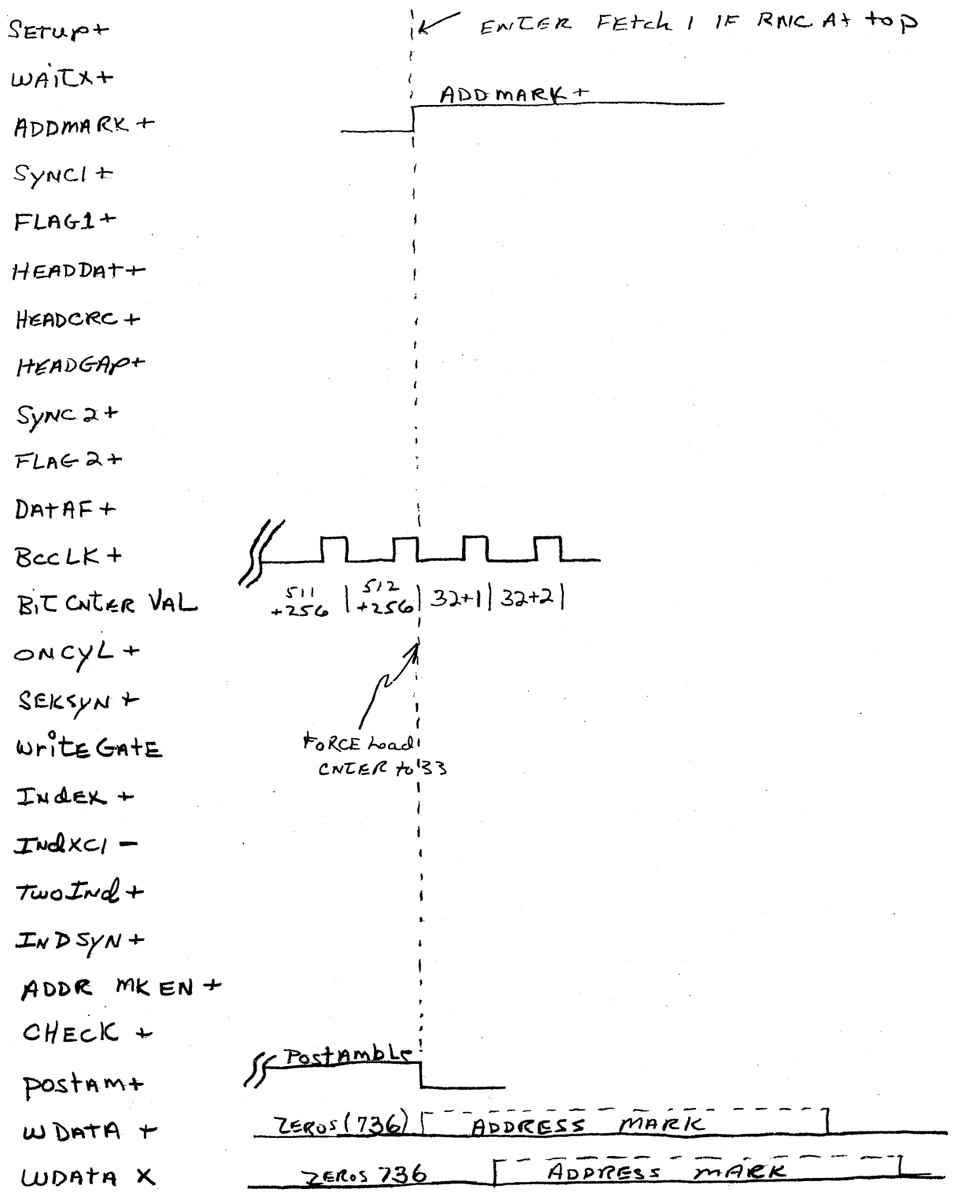
← Empty Followed by Fill →



FORMAT; SETup → postamble 1 OF 3



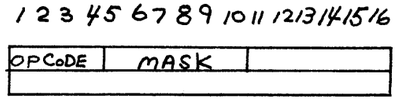

SEtup +
WAit +
ADD MARK +
SyNC1 +
FLAG1 +
HEAD DAT +
HEAD CRC +
HEAD GAP +
SyNC2 +
FLAG2 +
DATAF +
BccLK +
BiTCNTRVAL
ON CyL +
SEKSyN +
WRite Gate
INdEX +
INDXC1 −
TwoInd+
INDSyN+
ADDR MK EN +
CHeck +
PostAM +
WDATA +
WDATA X (X = 0→3)
HEAD DAT
HEAD CRC
HEAD GAP
SYNC 2
FLAG 2
DATAF +
+1 Record ADDRESS REG
RELoad REC ADD HEADER REG. OVER SYNC 2. ALSO RECord SIZE REG
31 | 32 | 33
47 | 48 | 49
52 | 53
256 | 8
15
0
31 | 32
PRESET TO (8)
CLEAR
check
PostAmble
WRITE HEADER
WRITE HEADER CRC
ZEROS
ONES
DATA Field OF ONES
WRITE DATA CRC
WRITE HEADER
WRITE HEADER CRC
ZEROS
WRITE DATA CRC


SETUP+
WAITX+
ADDMARK+
SYNC1+
FLAG1+
HEADDAT+
HEADCRC+
HEADGAP+
SYNC2+
FLAG2+
DATAF+
BCCLK+
BITCNTER VAL
ONCYL+
SEKSYN+
WRITEGATE
INDEX+
INDXC1-
TWOIND+
INDSYN+
ADDR MK EN+
CHECK+
postam+
WDATA+
WDATA X
ENTER FETCH 1 IF RNC AT top
ADDMARK+
511 +256
512 +256
32+1
32+2
FORCE load CNTER to '33
Postamble
ZEROS (736)
ADDRESS MARK
ZEROS 736
ADDRESS MARK

SMD CHANNEL INSTRUCTION SUMMARY

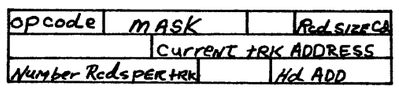
op Code

0 HALT



Stop CHANNEL program, AND UNbusy CONTROL UNIT

2 FORMAT



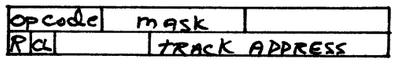
Rcd Size Code; DEFINES the LENGTH OF the DATA Field According to TABLE 1 IN Product Spec [USUALLY "0" FOR 1040 char RECord SIZE]

Current TRK ADDRESS; EQUAL to the ADDRESS OF the LAST SEEK order

NUMBER OF RECORD PER TRK; EQUAL to the Number OF RECords per REVOLUTION OF Disk must CORRESPOND to Rcd SIZE Code According to table 1

HEAD Address; DEFINES DATA Hd, maximum OF 19 FOR 300 mb, MAX 5 FOR 80 mb.

3 SEEK

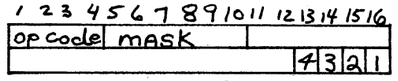


BIT 17; IF SET POSITIONER WILL do A RETURN TO ZERO SEEK (RECAL SEEK) AND TRACK ADDRESS WILL be ignored.

BIT 18; IF SET, the SELECTED DISK FILE WILL be CLEARED OF FAULTS IF the FAULT CONDITION NO LONGER EXISTS.

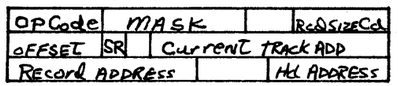
TRACK ADDRESS; MAX TRACK ADDRESS OF $823_{(10)}$ ($1467_{(8)}$) CYLINDERS ON 300 AND 80 mb. UNITS

4 Select



Select ONE OF Four MHD DEVICES by Setting the appropriate bit. the DEVICE WILL Remain SELECTED UNTILL deselected

5 Read
6 WRITE



Record Size Code; Code From table 1 INFORMS the CONTROLLER The Size OF the Data Field ("0" For a 1040 char Record)

OFFSET; Field is NORMALLY Zero AND IS USED FOR ERROR Recovery

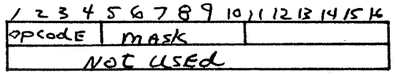
Short READ; IF A "1" ALLOWS the First part OF a RECORD to be read. USED to Locate the rotational POSITION OF DISK PACK.

TRACK ADDRESS; Set to the track address OF the Last Seek order.

Record ADDRESS; INDICATES the RECORD Number that the INSTRUCTION WILL operate ON with MAXIMUM VALUE determined by table 1

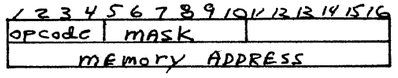
Head ADDRESS; DEFINES the Head that the Read OR write order WILL operate ON.

7 STALL



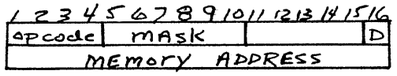
The STALL INSTRUCTION when EXECUTED will delay the CONTROL UNIT for 210 u sec before FETCHING the NEXT CHANNEL order.

9 INPUT STATUS



used to input CONTROLLER status to MEMORY LOCATION SPECIFIED in the SECOND WORD OF the INSTRUCTION

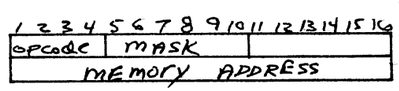
A Store



A store INSTRUCTION will Load ONE LOCATION OF the 64 LOCATION RAM IN the CONTROL UNIT, From the MAIN MEMORY LOCATION SPECIFIED IN the SECOND word OF the CHANNEL order.

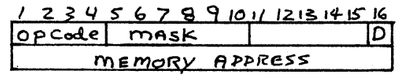
D; when this bit is A "0" the RAM ADDRESS REGISTER IS ALWAYS reset before it is used, So the INSTRUCTION will ONLY USE ONE LOCATION OF the RAM (Location "0"). IF A "1" the Address REG IS NOT reset, therefore you CAN write into or READ out of SUCCESSIVE RAM LOCATIONS.

B INPUT OAR



INPUT the CONTENTS OF the ORDER ADDRESS REGISTER TO the LOCATION SPECIFIED by word two OF the ORDER. ALWAYS the LOCATION OF the INSTRUCTION PLUS two.

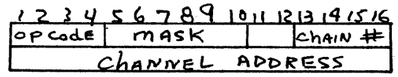
C LOAD



this ORDER does the opposite OF A STORE order. the Load order takes the CONTENTS OF ONE LOCATION IN the RAM AND STORES IT IN the MEMORY LOCATION SPECIFIED IN word two OF the order.

D; SEE STORE ORDER FOR EXPLANATION.

D CHAN ADD

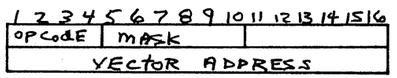


this order INFORMS the CONTROLLER which DMA CHANNELS WILL be used FOR DATA TRANSFER AND HOW MANY ARE to be CHAINED

CHAIN NUMBER; the NUMBER OF CONSECUTIVE CHANNELS to be USED beyond ONE.

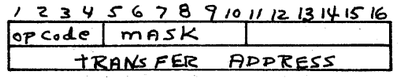
CHANNEL ADD; the FIRST DMA CHANNEL to be USED

E INTERRUPT



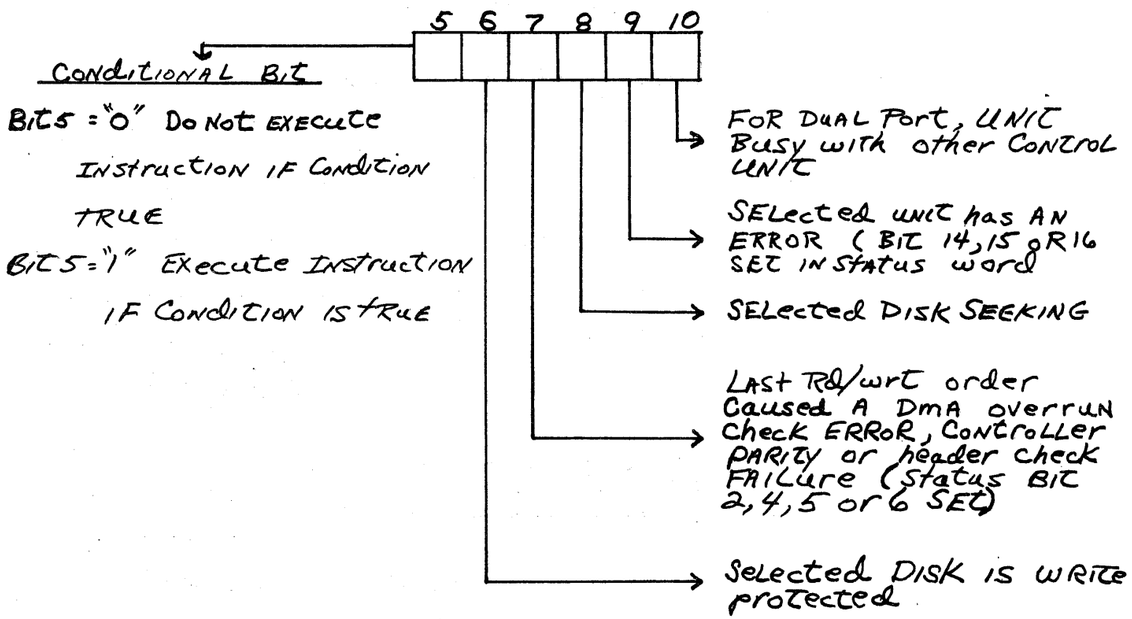
when this order is executed AN I/O BUSS INTERRUPT is generated by the CONTROLLER. ALL CHANNEL processing STOPS UNTILL AN OCP 16 IS received by the CONTROLLER. the VECTORED ADDRESS must be SPECIFIED AS there IS NO DEFAULT Address.

F TRANSFER



Execution of this order will Replace the Contents of the ORder ADDRESS REGister with the Contents of the Second word of the INSTRUCTION. the TRANSFER order is SIMILAR to A CPU JUMP INSTRUCTION EXCEPT A CONDITION CAN be SPECIFIED by the MASK bits.

MASK BITS



CHANNEL program Example

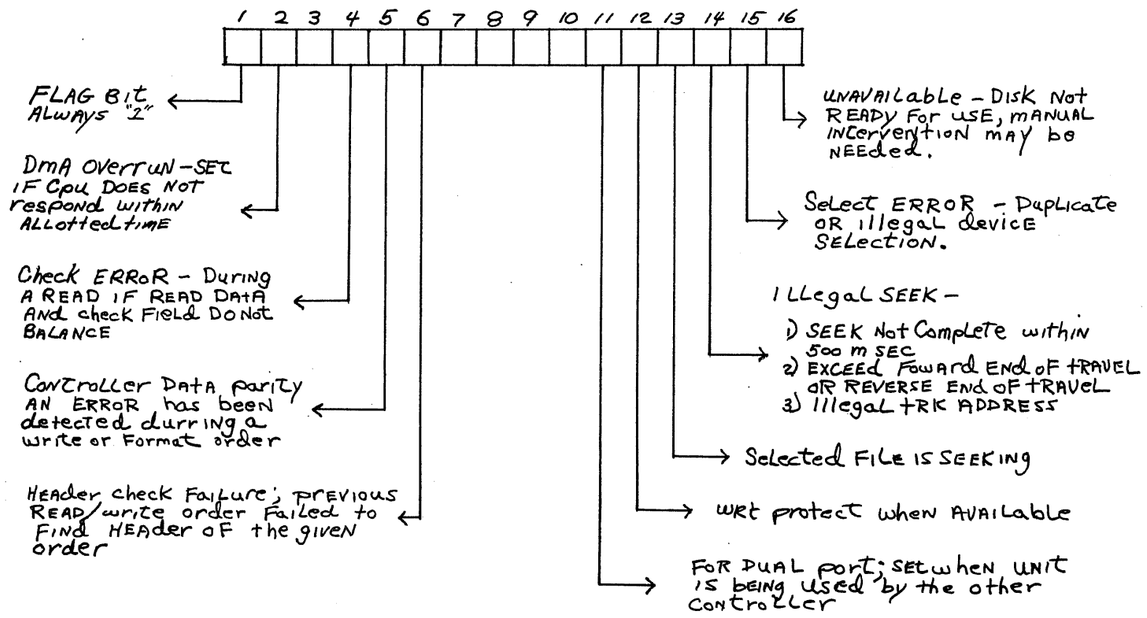
Typical repetitive SEEK

```
OCP 1726          ──────────→  SEL
LDA (prog ADD)                 SEEK
OTA 1726   START Chan Prog     XFER (IF SEEKing)
                               SELF
Jmp -1                         SEEK
INA 1726  } Loop on INA Should
Jmp -1    } NEVER HLt.         XFER (IF SEEKing)
                               SELF
HALT                           XFER (to First SEEK)
```

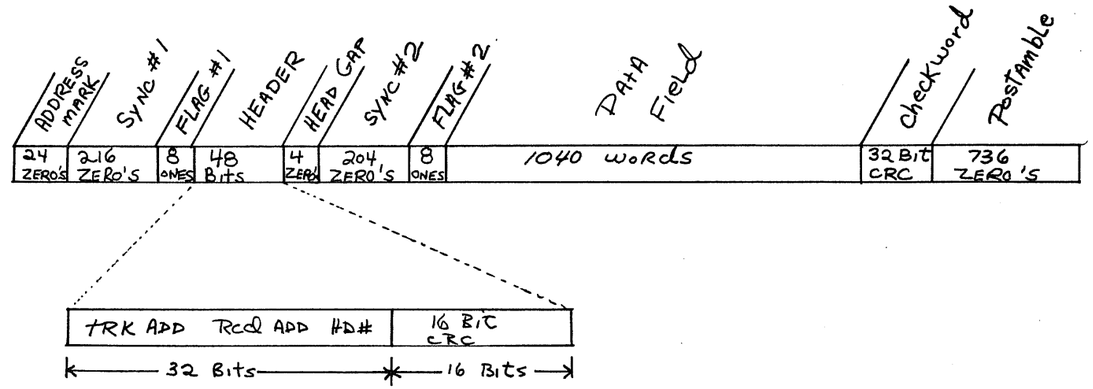
Typical READ ORDER

```
OCP 1726          ──────────→  SEL
LDA (prog ADD)                 SEEK
OTA 1726   START CHAN PROG     Chan ADD
                               READ
Jmp -1                         Input stat
INA 1726  } Should Loop here
Jmp -1    } until CHN prog     HLt
              HLts then skip
HALT
```

STATUS WORD



SMD RECORD



LTR	DATE	REVISION	DR.	CK.
		RELEASED PER ECR 1774-A (I... W.L. REV 1 FILE NAME WWESL1)		
	5/4/76	RELEASED AT W.L. REV 4		
	5/26/76	PER ECR 1774-A W.L. REV 5 WL REV 6 ECR 1807		
	6/7/76	WIRE LIST TO REV 7 PER ECR 1818		
	7-30-76	PER ECR 1840 WIRE LIST TO REV 8		
	11-3-76	PER ECR 1946		
	12-28-76	PER ECR 1975 WIRE LIST TO REV 9		
	12-30-76	REMOVED JC DESIGNATION AT 27M PER ECR 1928		
	4-11-77	REVISED PER ECR 2153 WIRE LIST TO REV 10		

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

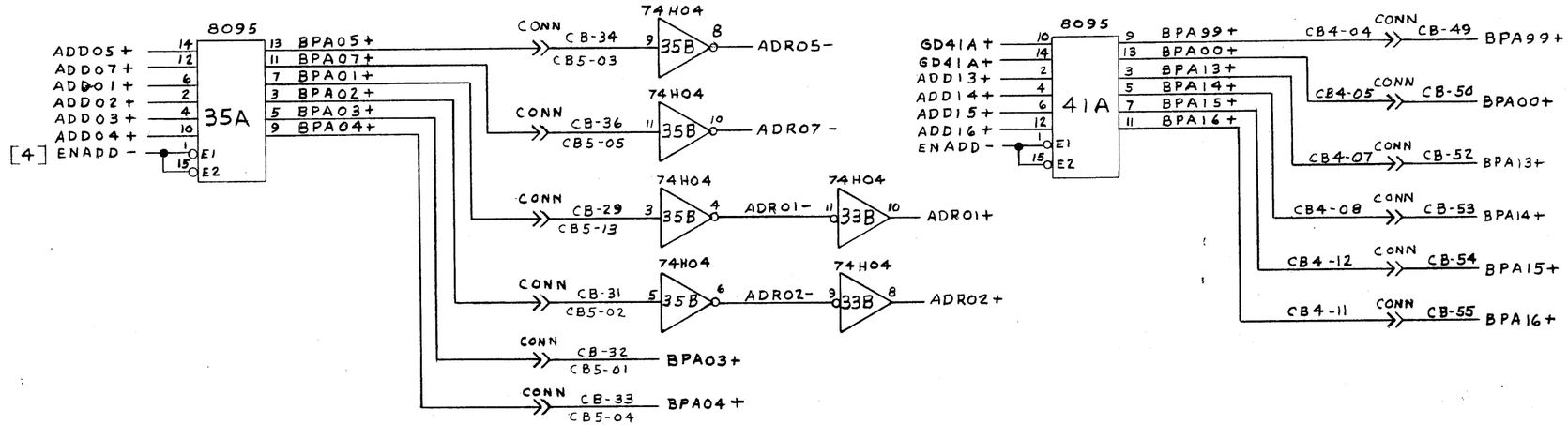
NOT USED

REVISION LEVEL

6R-2

MATERIAL	DWN W. Tagyan 2/9/76	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED – REMOVE ALL BURRS AND SHARP EDGES: – DIMENSIONS ARE IN INCHES – TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG. 5/4/76 Derek J. Gardner	REVISION STATUS SHEET STORAGE MODULE CONTROLLER 4004	
	APPRD		
	USED ON 4004-901 NEXT ASSY ESA 2060-901	SCALE SHEET 1 OF 42	SIZE C DWG. NO. LBD 2437 REV.

II-01



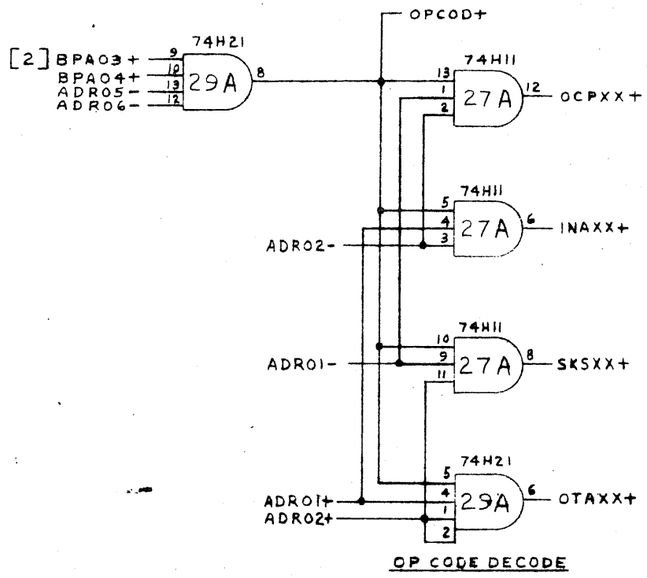
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD-!- +		
MODE0 +		
MODE1 +		
MODE2 +		
MODE3 +		
MODE4 +		

I/O BUS ADDRESS
DRIVERS & RECEIVERS

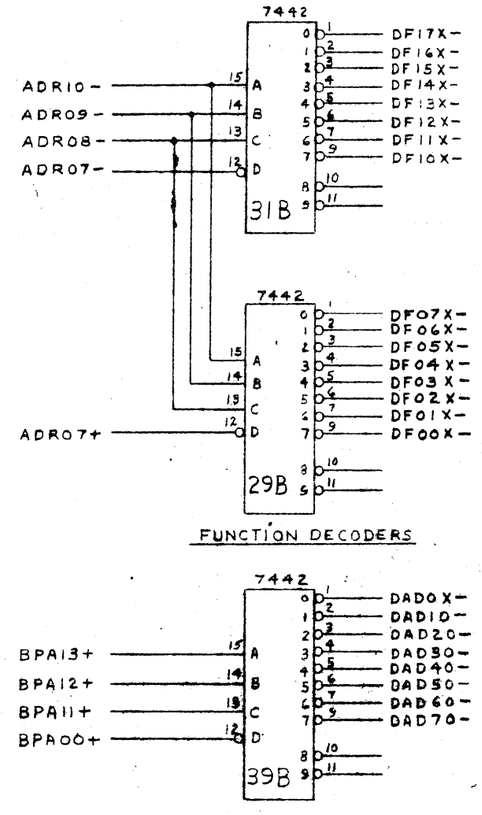
II-02

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS AND MODE LINES WW III	
	ENG.		
	APPRD		
USED ON NEXT ASSY	SCALE SHEET 2 OF	SIZE C	DWG. NO. LBD 2437 REV. B

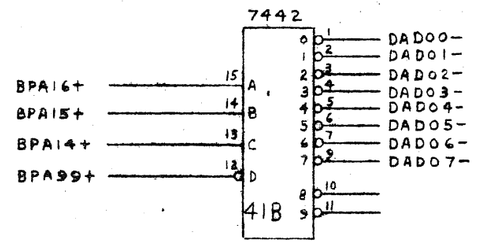
PDF-003



OP CODE DECODE



FUNCTION DECODERS



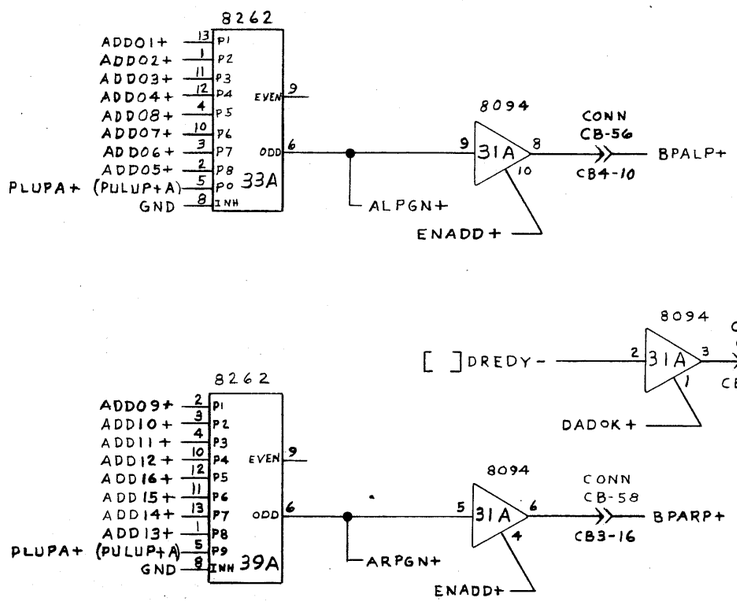
OCTAL ADDRESS DECODERS

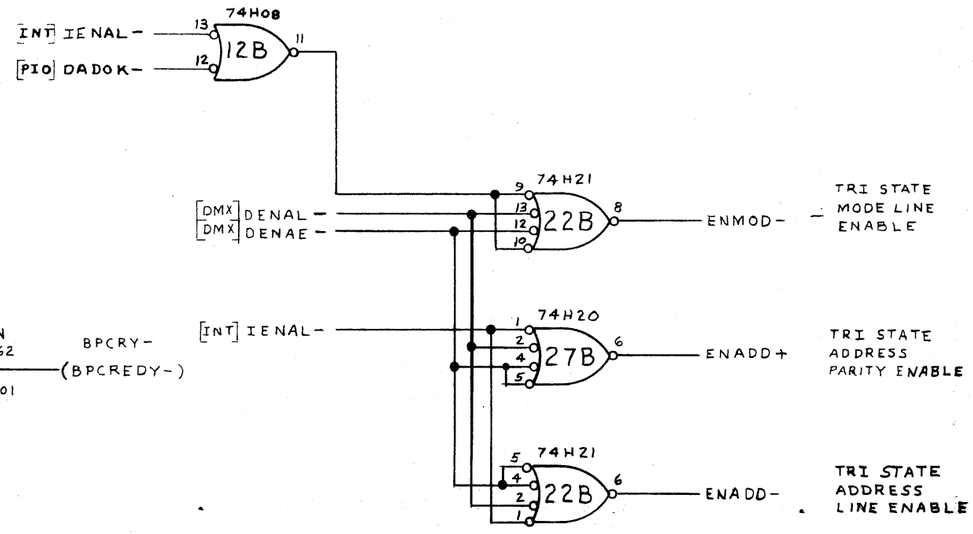
MATERIAL	DRN W. Bogan 3/14/74	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES; — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ±.02, .XXX ±.005, ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS DECODING WW III
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF
		SIZE C · DWG. NO. LBD2437 · REV. A

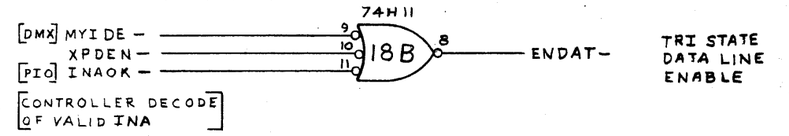
II-03

PDF-003

PRIME COMPUTER, INC.

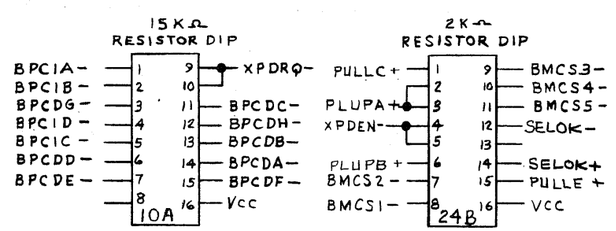






CONN		
BMCS1- (BMCEXS1-)	CA2-11	CA-87
BMCS2- (BMCEXS2-)	CA2-09	CA-89
BMCS3- (BMCSS01-)	CA1-15	CA-91
BMCS4- (BMCSS02-)	CA1-13	CA-93
BMCS5- (BMCSS03-)	CA1-02	CA-95
BPCFC+ (BPCFCLK+)	CA1-01	CA-90
BPCSC+ (BPCSCLK+)	CB1-14	CB-90
HPRFL- (HPWRFL-)	CB6-09	CB-25

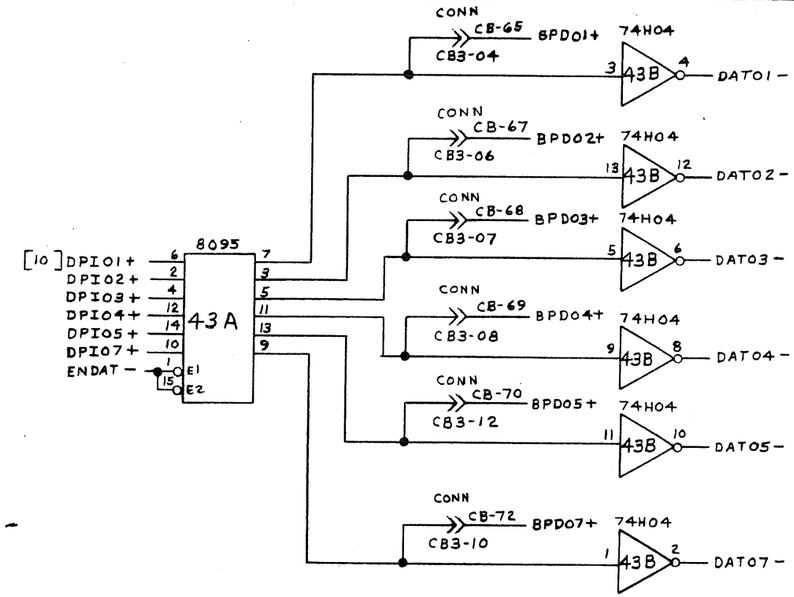
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
COCMD+		
ADD__+		
DADOK-		
XPMOD-		
XPDEN-		
INAOK-		
OTAOK+		
XPDEE-		
DREDY-		
DADOK+		

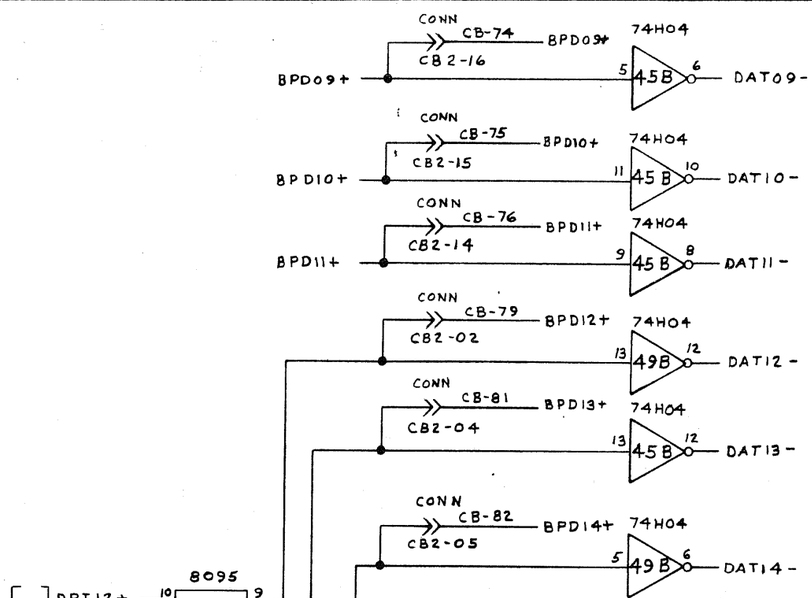


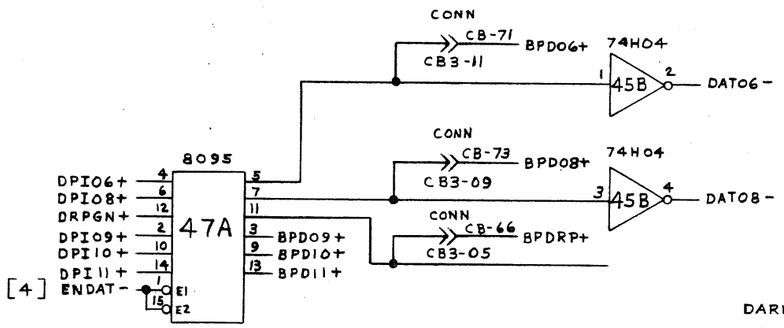
MATERIAL	DWN W Ingram 3/4/74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK ENG. APPRD USED ON NEXT ASSY	I/O BUS INTERFACE LOGIC ADDRESS PARITY WW III	
		SCALE SHEET 4 OF	SIZE C DWG. NO. LBD2437 REV. C

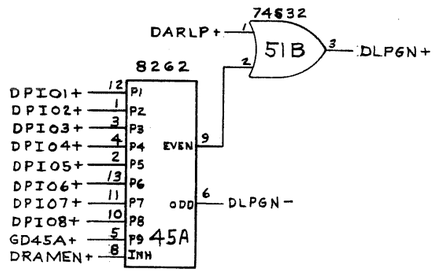
II-04

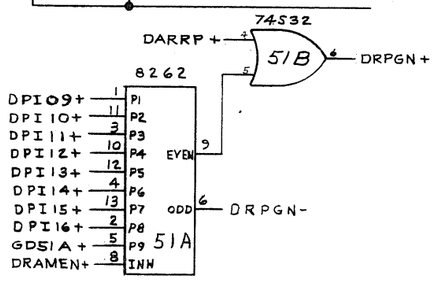
PRIME COMPUTER, INC.











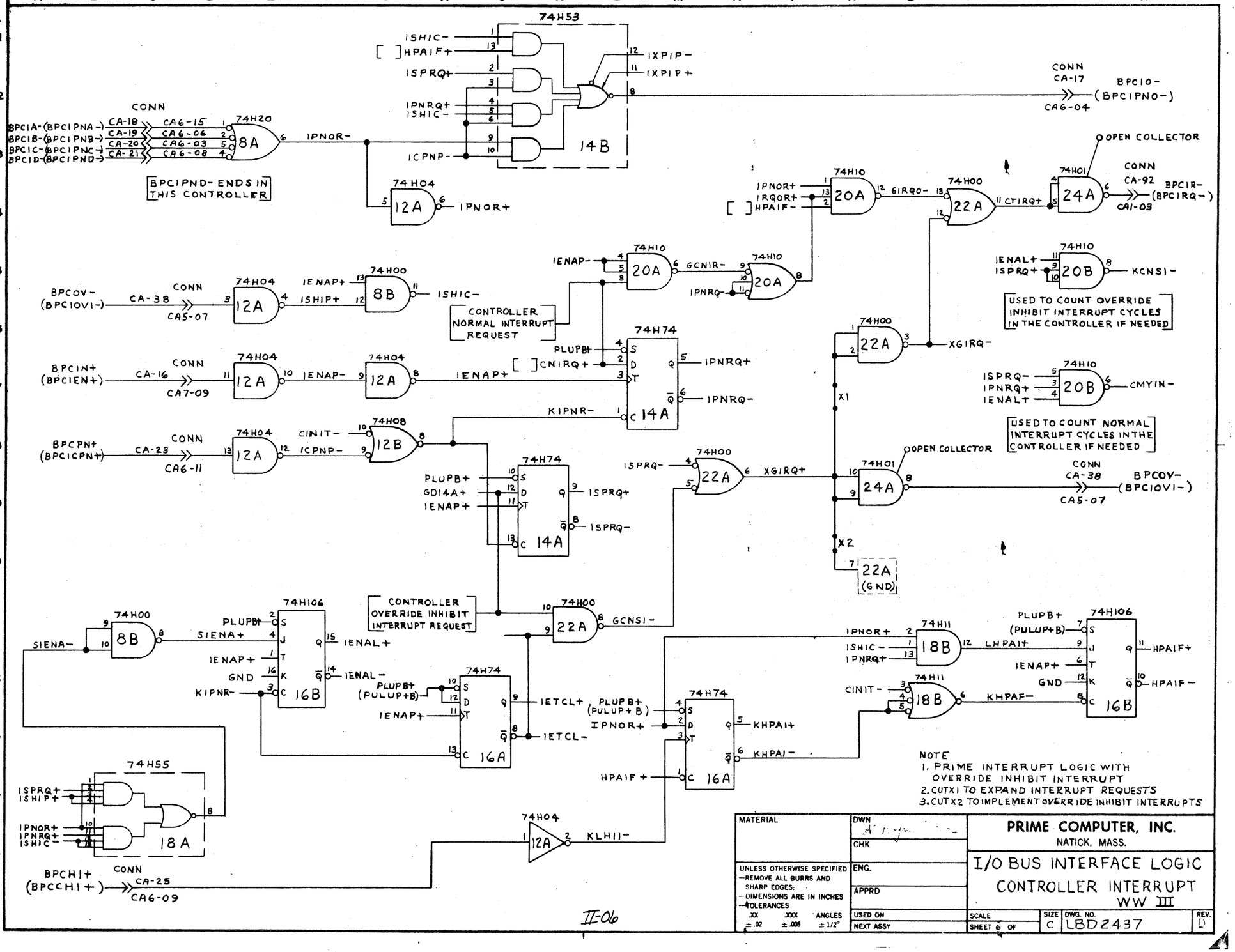
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
DPI +		

MATERIAL	DWN [illegible] 3/5/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	I/O BUS INTERFACE LOGIC DATA BUS LINES WW III
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 5 OF — SIZE C — DWG. NO. LBD 2437 — REV. B

II-05

PDF-003

PRIME COMPUTER, INC.

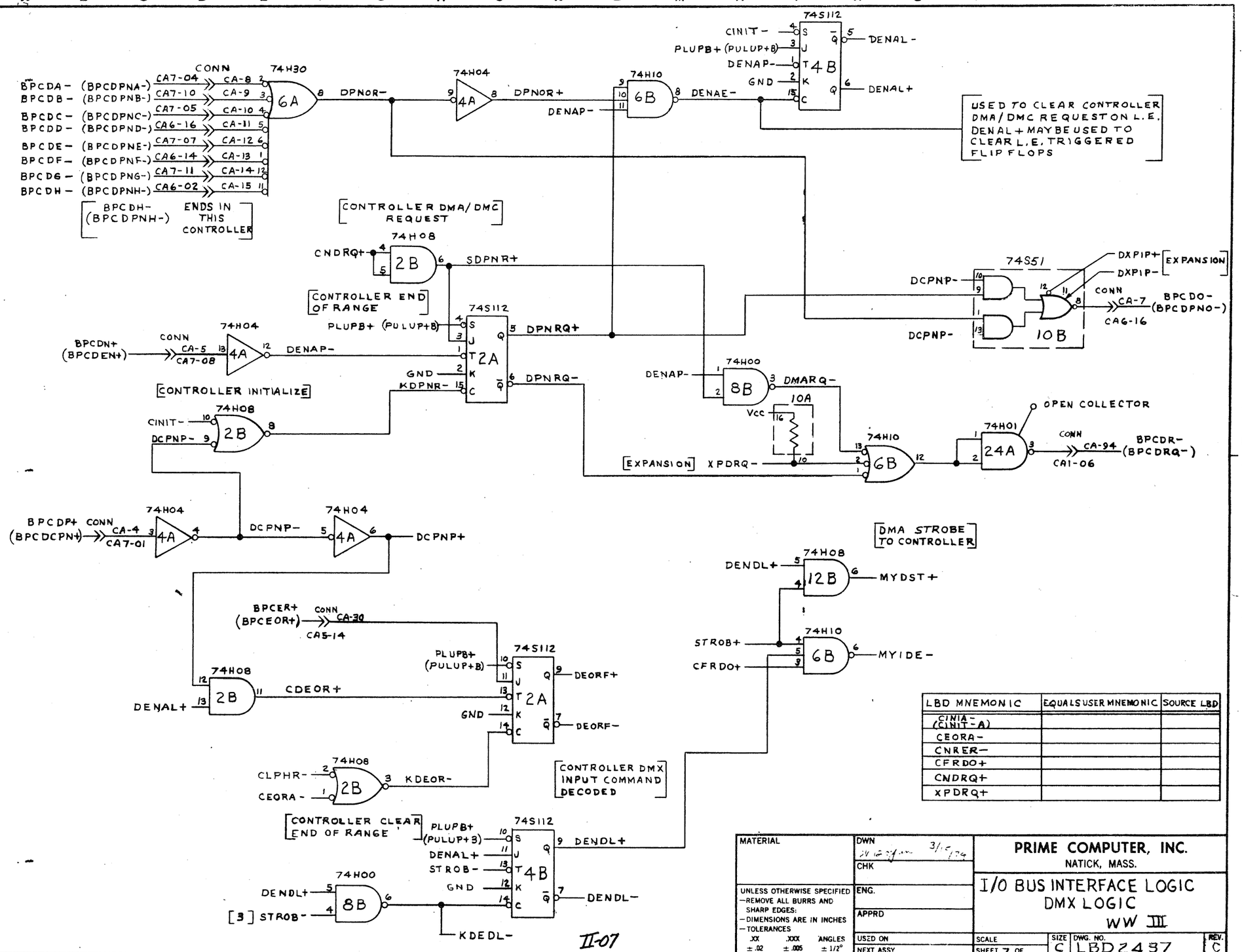


NOTE
1. PRIME INTERRUPT LOGIC WITH OVERRIDE INHIBIT INTERRUPT
2. CUTX1 TO EXPAND INTERRUPT REQUESTS
3. CUTX2 TO IMPLEMENT OVERRIDE INHIBIT INTERRUPTS

II-06

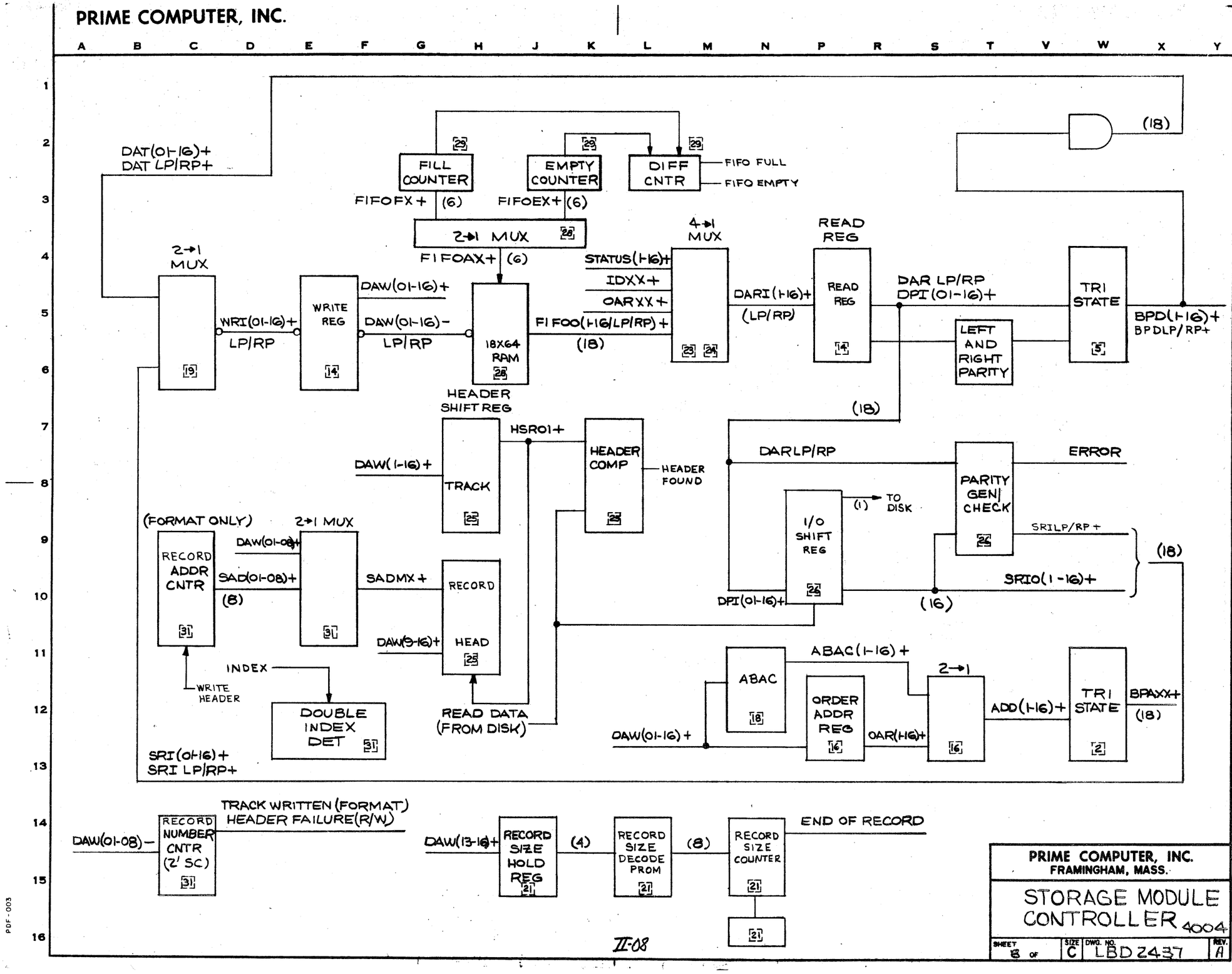
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	I/O BUS INTERFACE LOGIC CONTROLLER INTERRUPT WW III
	ENG.	
	APPRD	
USED ON / NEXT ASSY	SCALE / SHEET 6 OF	SIZE C / DWG. NO. LBD2437 / REV. D

PDF-003



LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIA- (CINIT-A)		
CEORA-		
CNRER-		
CFRDO+		
CNDRQ+		
XPDRQ+		

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC DMX LOGIC WW III
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 7 OF
		SIZE C / DWG. NO. LBD2457 / REV. C



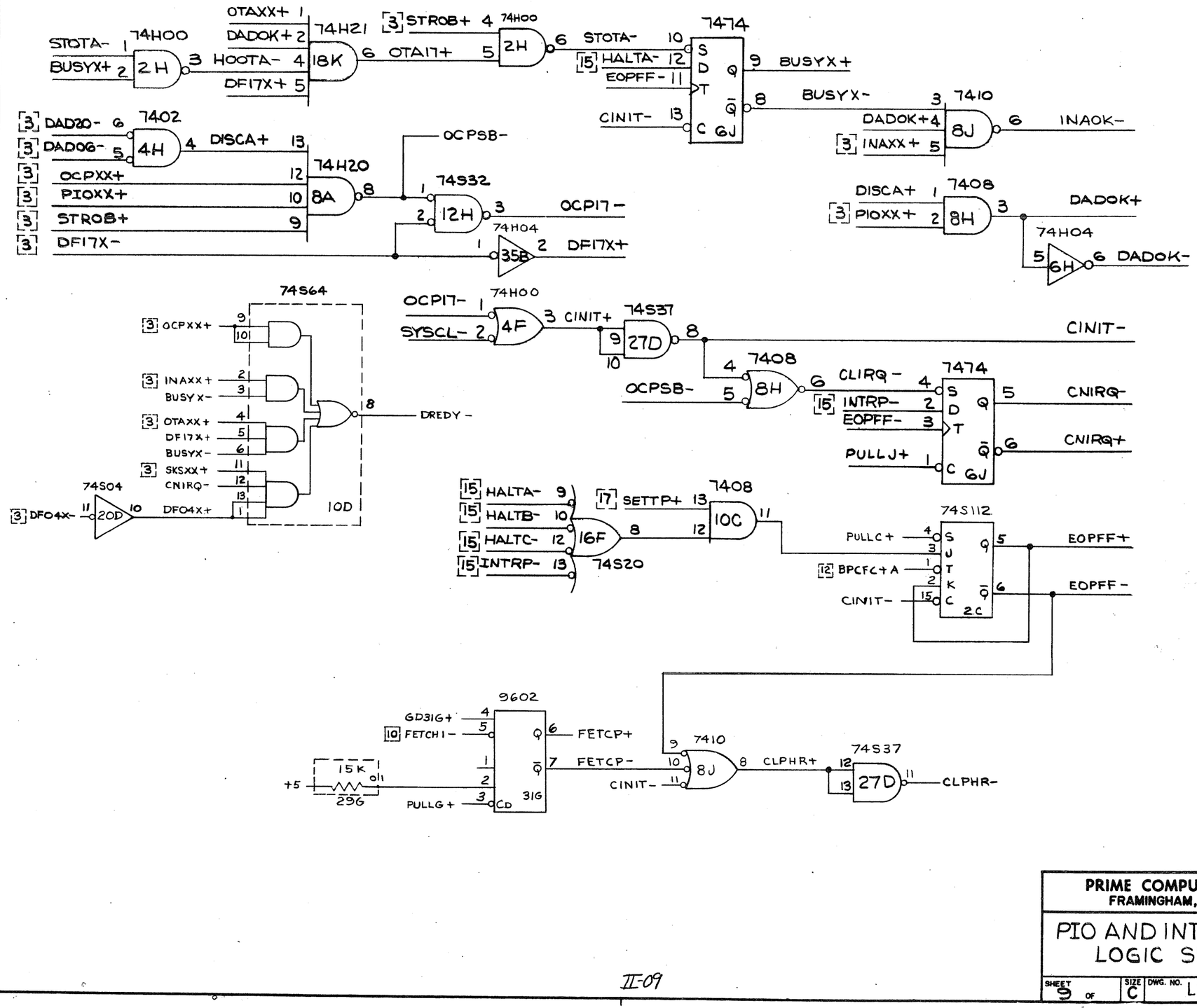
II-08

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

STORAGE MODULE CONTROLLER 4004

SHEET 8 OF | SIZE C | DWG. NO. LBD2437 | REV. A

PDF-003

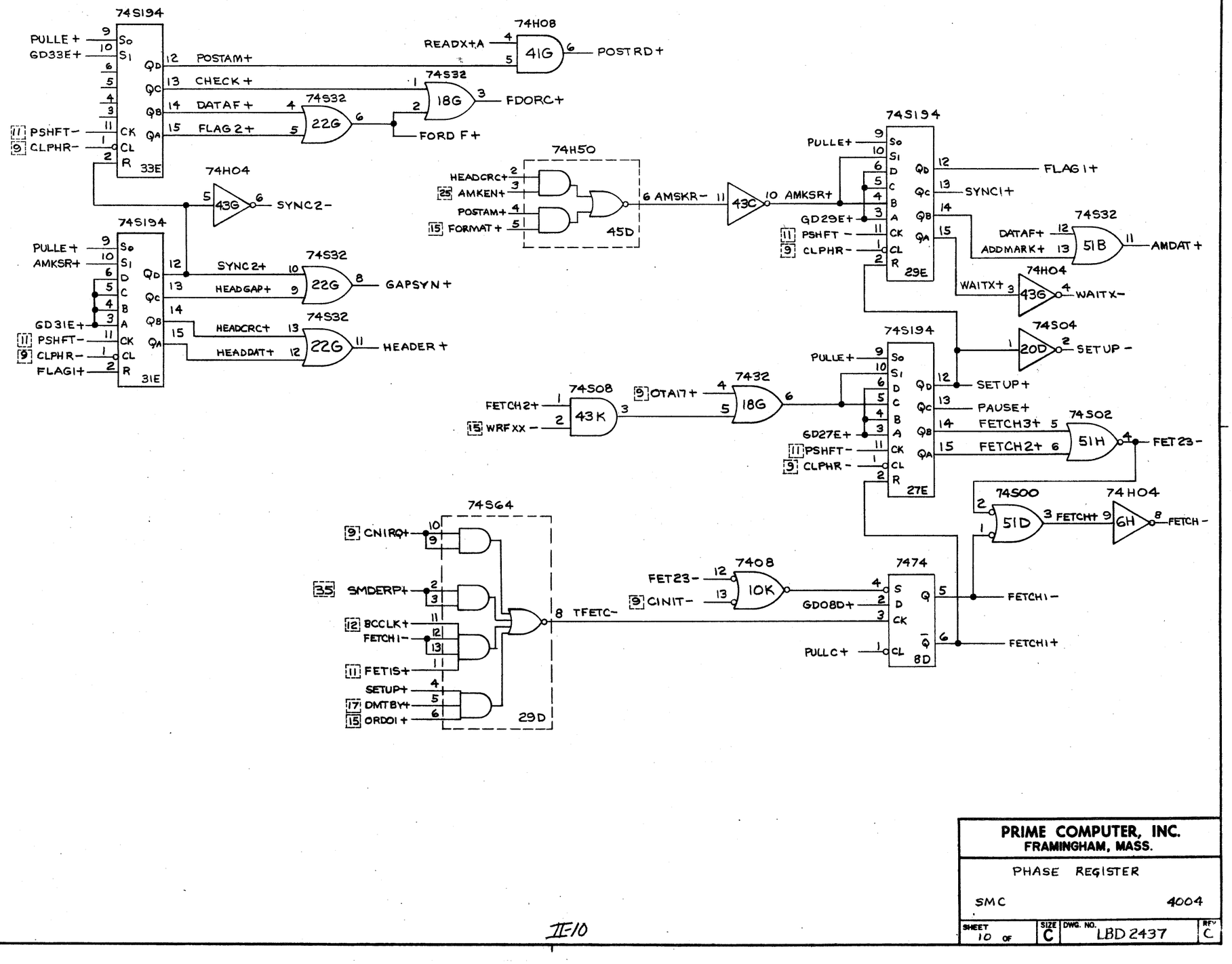


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

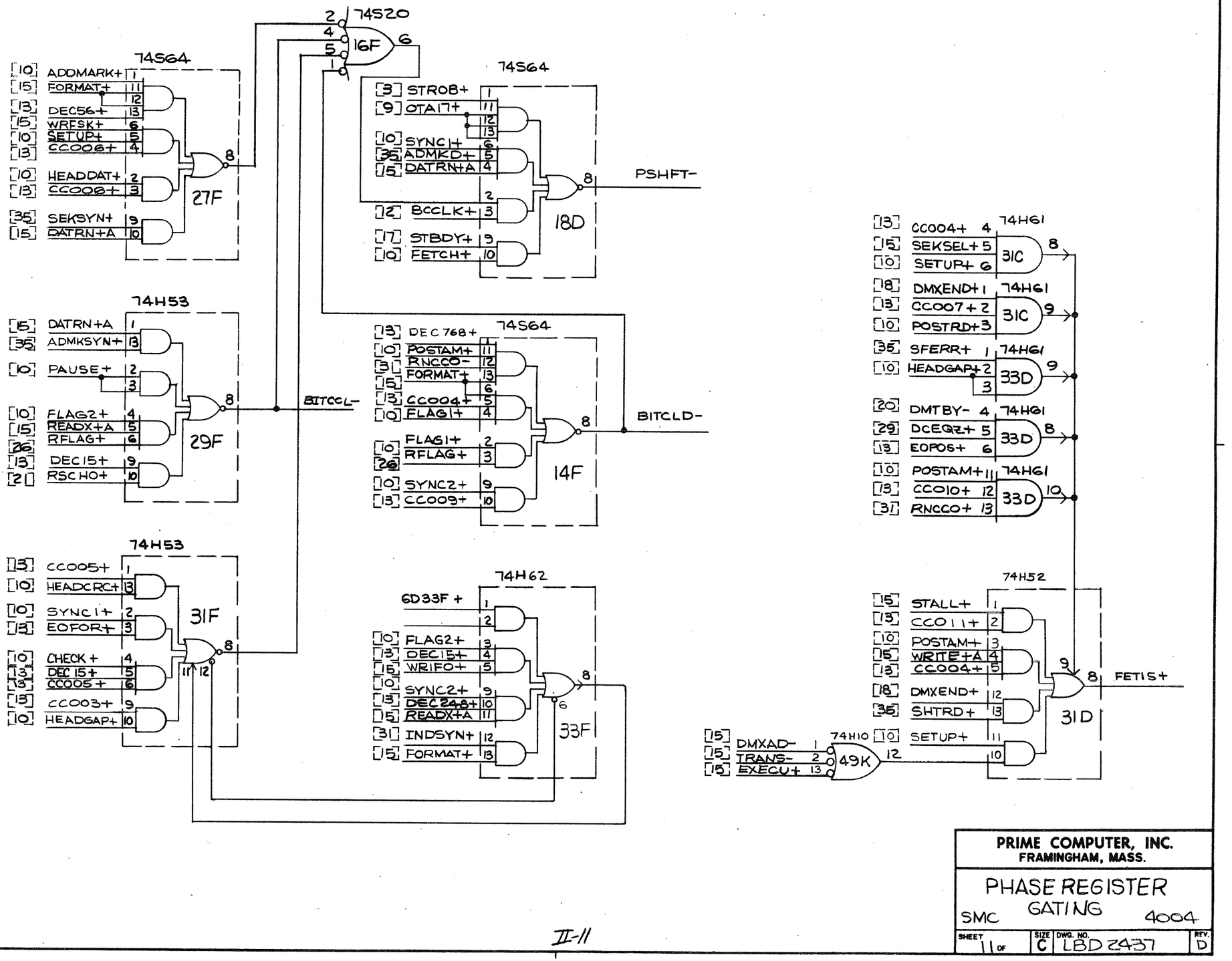
PIO AND INTERRUPT
LOGIC SMC 4004

SHEET 9 OF | SIZE C | DWG. NO. LBD2437 | REV. A

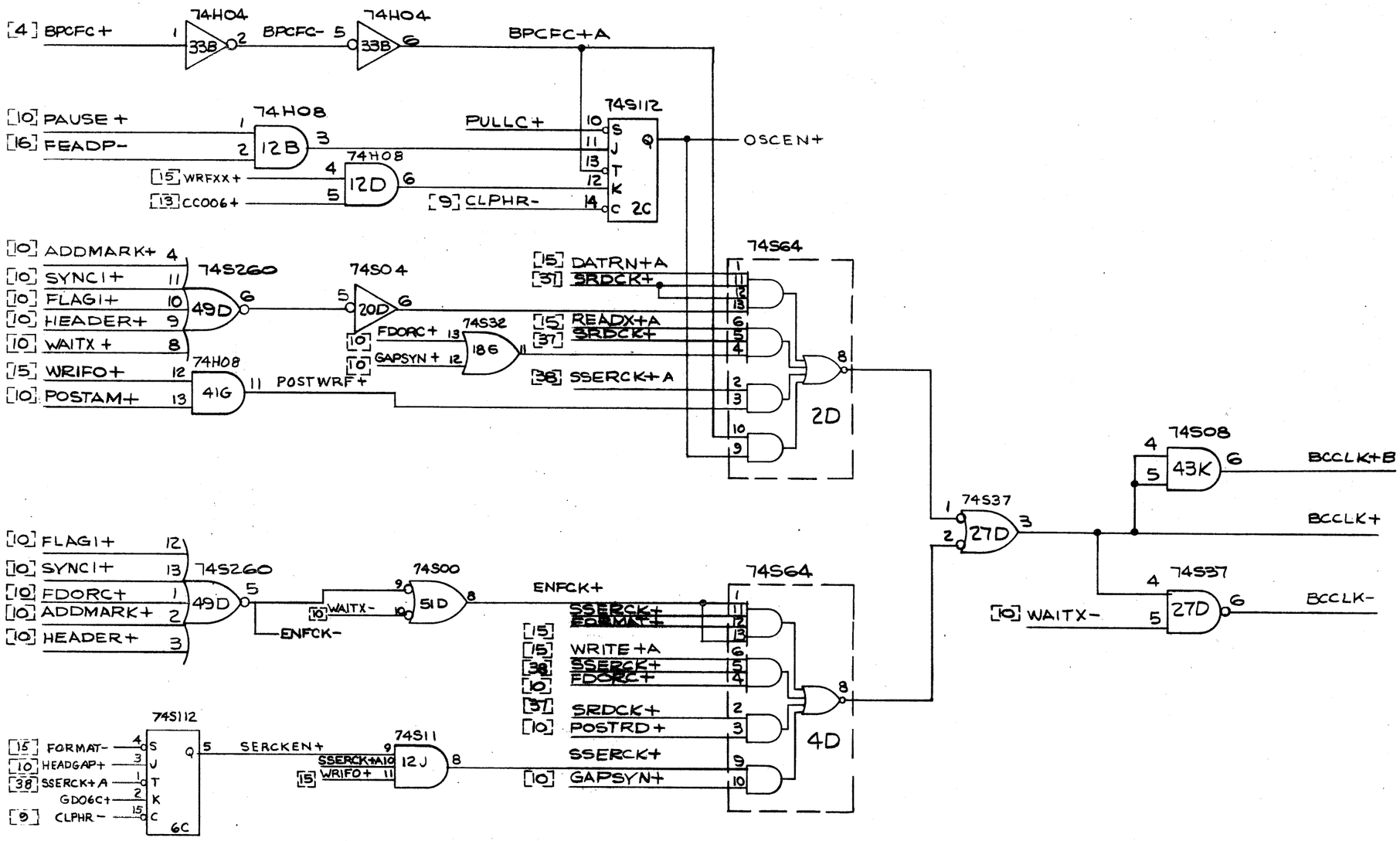
PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
PHASE REGISTER			
SMC 4004			
SHEET 10 OF	SIZE C	DWG. NO. LBD 2437	REV C



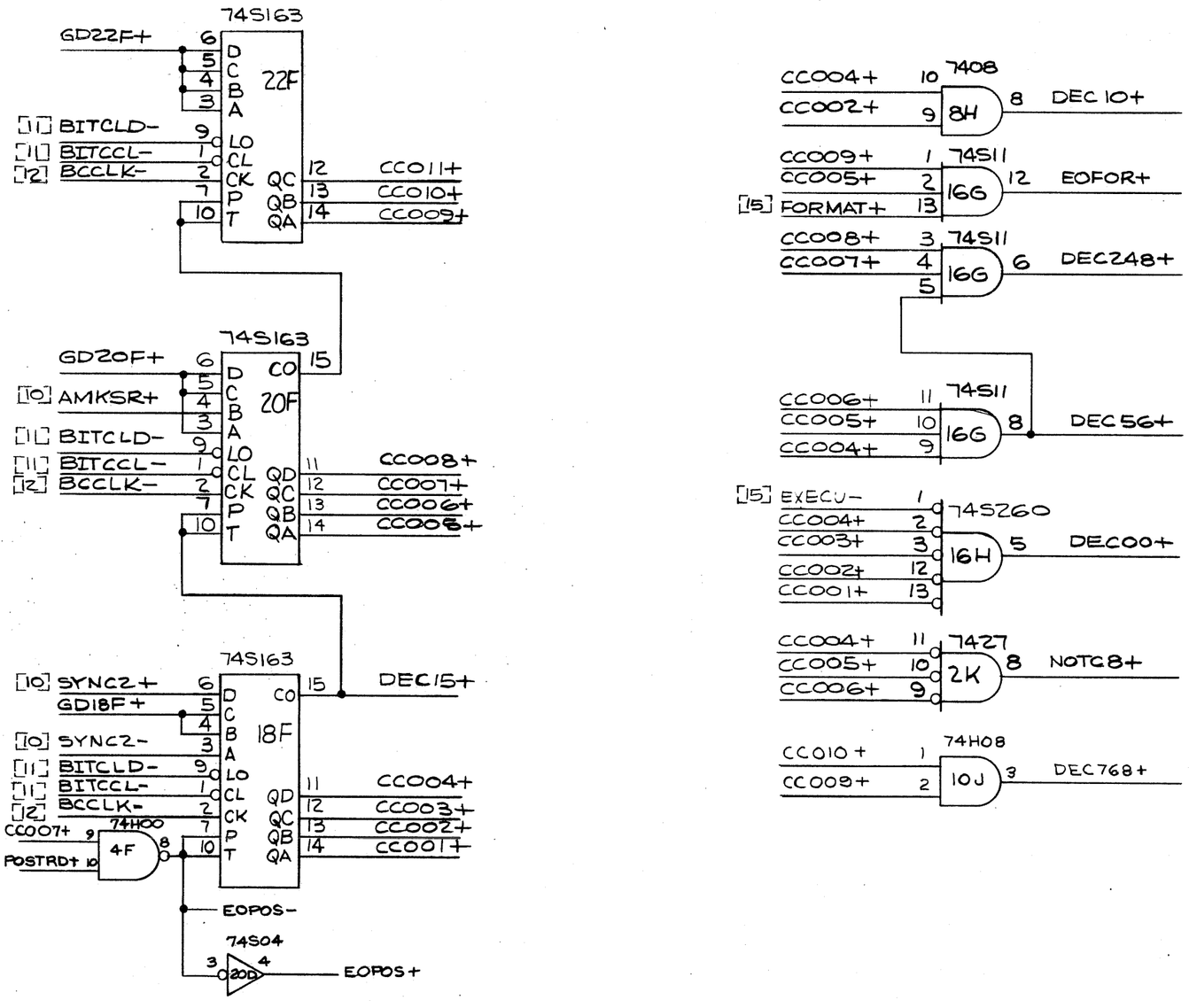
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
PHASE REGISTER SMC GATING 4004			
SHEET 11 OF	SIZE C	DWG. NO. LBD 2437	REV. D



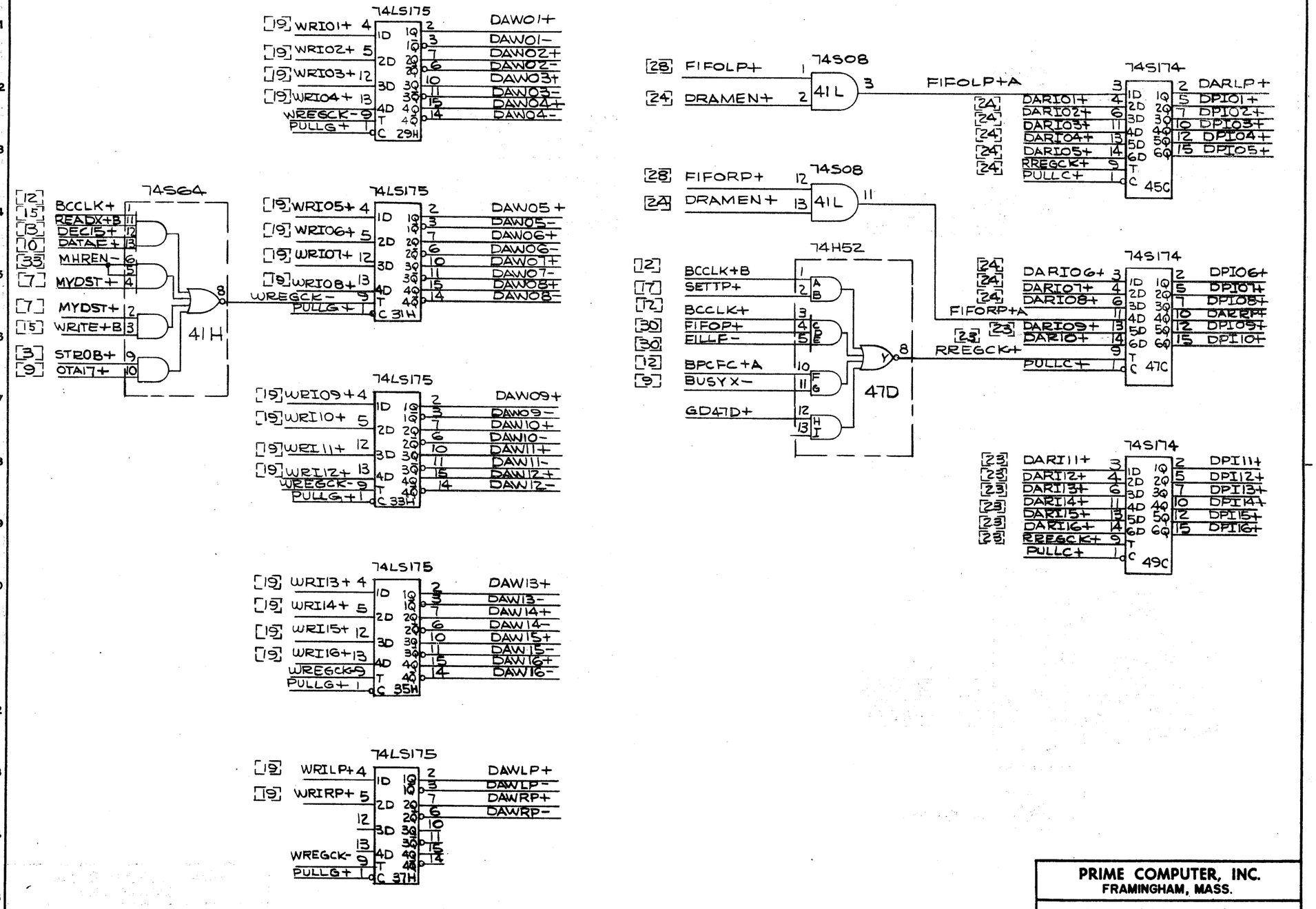
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	V	W	X	Y			

PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
CLOCK LOGIC	
SMC	4004
SHEET 12 OF	SIZE C / DWG. NO. LBD 2437 / REV. B

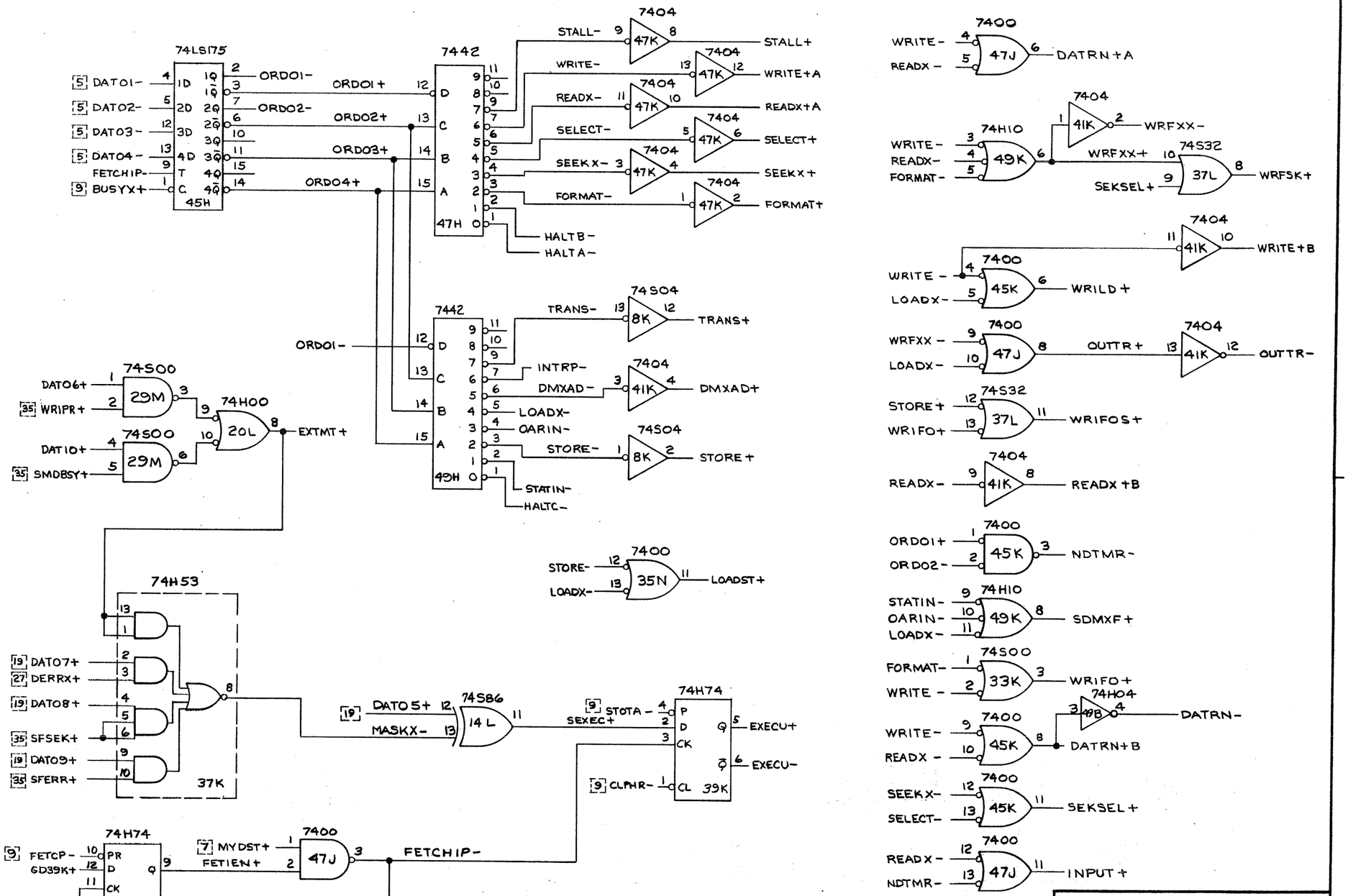
PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
BIT COUNTER	
SMC	4004
SHEET 13 OF	SIZE C / DWG. NO. LBD 2437 / REV. B



PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
WRITE AND READ REGISTERS SMC 4004	
SHEET 14 OF	SIZE C
DWG. NO. LBD 2437	REV. A

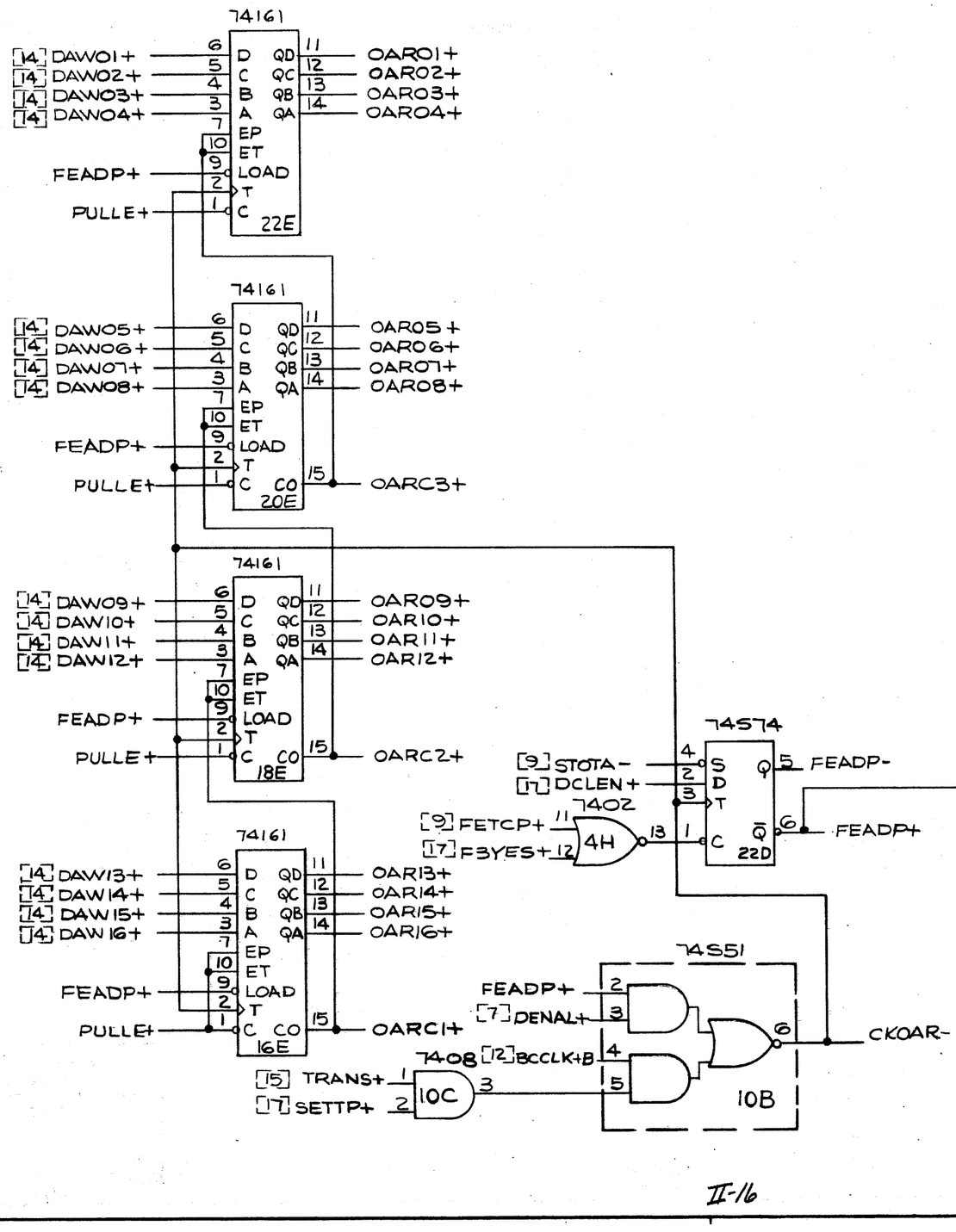


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ORDER REGISTER
AND MASK CONDITIONS

SMC 4004

SHEET	SIZE	DWG. NO.	REV.
15 OF	C	LBD 2437	B



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ORDER ADDRESS REG AND ADDRESS INPUT MPX

SMC 4004

SHEET 16 OF | SIZE C | DWG. NO. LBD2437 | REV. A

PDF-003

VCC29G+ GD29G+
29G
12 13
470Ω 390Ω
5 4
GD04E+
8 14
4E
200 NS DELAY
T1,T2,T3,T4
1 7
2 3 5 6
[7] MYDST+
DLYTO+
74S04
74S08
4 6
1 2 5
6F
35K
STBDY+
DLYT4-
DLYT4+
74H50
[7] CDEOR+
[17] DRCO2+
[9] CINIT+
2 3 4 5
2A 2B 2C 2D
6
10F
74S64
[10] AMDAT+
[29] DCLT56+
[5] WRITE+A
DMTBY-
[15] READX+A
DMTBY-
[29] DCGT7+
[5] STORE+
[30] FIFOP+
1 11 12 13 3 6 5 4 2 3 9 10
8
8G
74S02
8 9
22J
10
SDMTR+A
[12] BCCLK-
74S11
[10] SETUP+
[5] DECOO+
[13] NOTC8+
3 4 5
12J
6
SETTP+
[75] SDMXF+
74H08
[15] INPUT+
[10] FETCH-
10 9
12D
8
CFRDO+
74S64
[7] CDEOR+
DRCO1+
DRCO2+
DRCO4+
[10] FETCH-
[5] DATRN+A
[8] EOREOC+
[9] CINIT+
1 11 12 13 6 5 4 2 3 9 10
8
2F
74H52
[16] FEADP+
DRCO2+
DRCO1+
[16] FEADP+
GD02G+
[10] SETUP+
[15] WRITE-
1 2 3 4 5 10 11 12 13
A B C D E F G H I
Y
8
2G
DCLEN+
74S32
10 9
12H
8
[9] FETCP+
DRQCL-
SDMTR+
74H04
11
6H
10
SDMTR-
ADDRESS PHASE COUNTER
74161
PULLG+
9 7
LO P
2 1
CK CL
QC QB QA
12 13 14
DRCO4+
DRCO2+
DRCO1+
10G
SDMTR-
74S112
PULLG+
[15] WRFXX+
[10] FETCH1+
GD20H+
4 3 1 2 15
PR J CK K C
Q Q̄
5 6
F3YES+
20H
F3YES-
74S112
[35] SMDERR
GD02E+
10 11 13 12 14
S J T K C
Q Q̄
9 7
CNDRQ+
CNDRQ-
2E
[7] DENAL+
5
41K
6
DENAL-A
7404

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

DMA REQUEST
SMC LOGIC 4004

SHEET 17 OF | SIZE C | DWG. NO. LBD 2437 | REV C

PDF-003

PRIME COMPUTER, INC.

ADDRESS BUS ADDRESS COUNTER

74161

[14] DAW01+
[14] DAW02+
[14] DAW03+
SETUP-
PULLE+
ABAC01+
ABAC02+
ABAC03+
14E

74H50

[7] DEORF+
[5] DATRN+A
[12] BCCLK+B
ABACCK-
6D

7408

[5] ORD01+
[17] SETTP+
ABACLD+
10C

74H11

[5] DATRN+A
[7] DENAL+
MODE1+
45G

7400

[16] FEADP-
[10] SETUP-
4C

7408

MODE0+
10C

74H08

[7] DENAL+
[17] CFRD0+
MODE4+
12D

74161

[14] DAW04+
[14] DAW05+
[14] DAW06+
[14] DAW07+
SETUP-
ABACCK-
PULLE+
ABAC04+
ABAC05+
ABAC06+
ABAC07+
ABACC2+
12E

74161

[14] DAW12+
[14] DAW13+
[14] DAW14+
[14] DAW15+
PULLE+
SETUP+
ABACCK-
PULLE+
ABAC12+
ABAC13+
ABAC14+
ABAC15+
ABACCO+
8E

74161

[14] DAW08+
[14] DAW09+
[14] DAW10+
[14] DAW11+
SETUP-
ABACCK-
PULLE+
ABAC08
ABAC09
ABAC10
ABAC11
ABACC1+
10E

7474

PULLC+
DAW16+
ABACLD+
[12] BCCLK+B
LSBCK-
7400
14D
ABAC16+
8D

74161

[14] DAW13-
[14] DAW14-
[14] DAW15-
[14] DAW16-
[10] FETCH1-
PULLC+
CHNCK-
EOCXX+
14C

74H50

[7] DEORF+
[2] FETIP+
[15] DMXAD+
6D

7400

[7] DEORF+
14D
EOREOC-

74S02

DMTBY+
22J
DMXEND+

74S04

20D
EOREOC+

7432

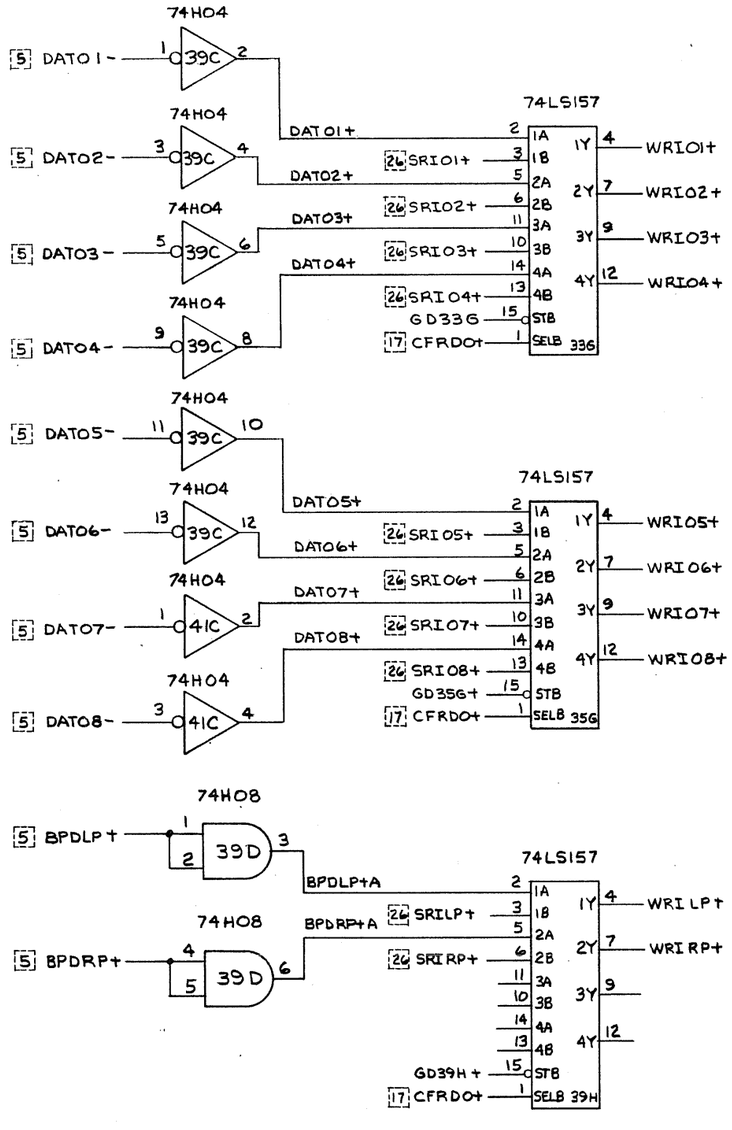
[7] DENAP-
51B
CEORA-

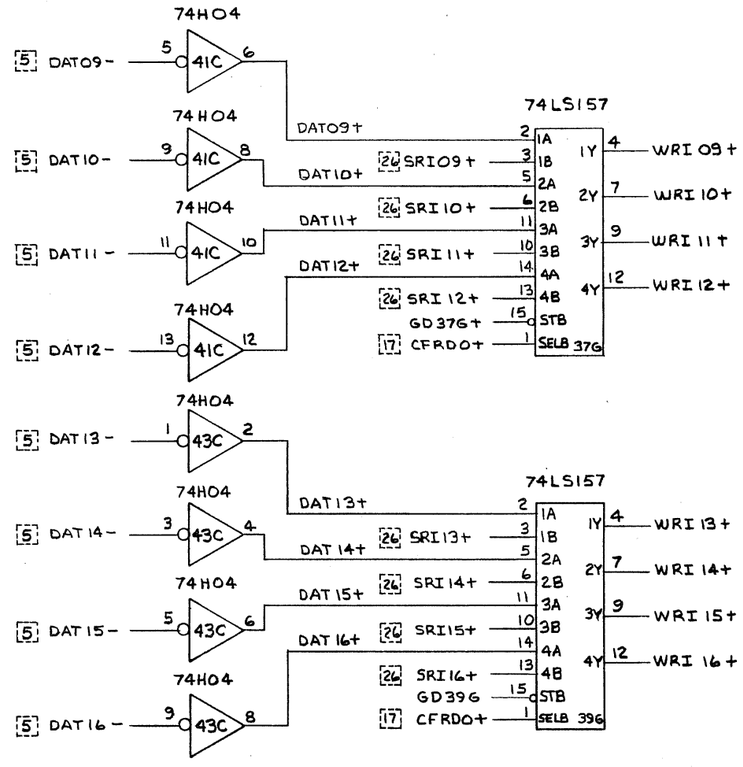
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

DMA CHANNEL AND CHAIN

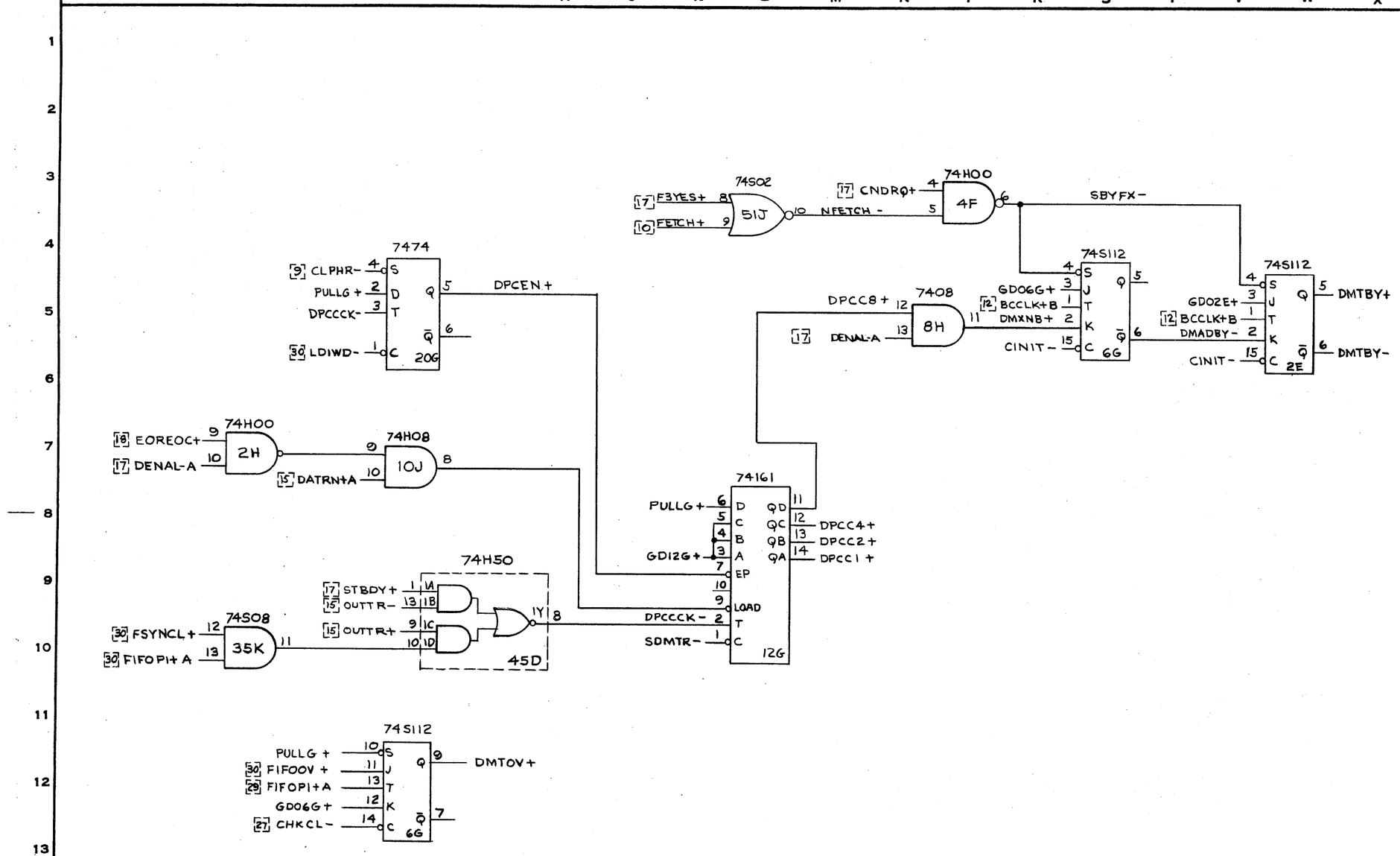
SMC 4004

SHEET 18 OF | SIZE C | DWG. NO. LBD2437 | REV. A

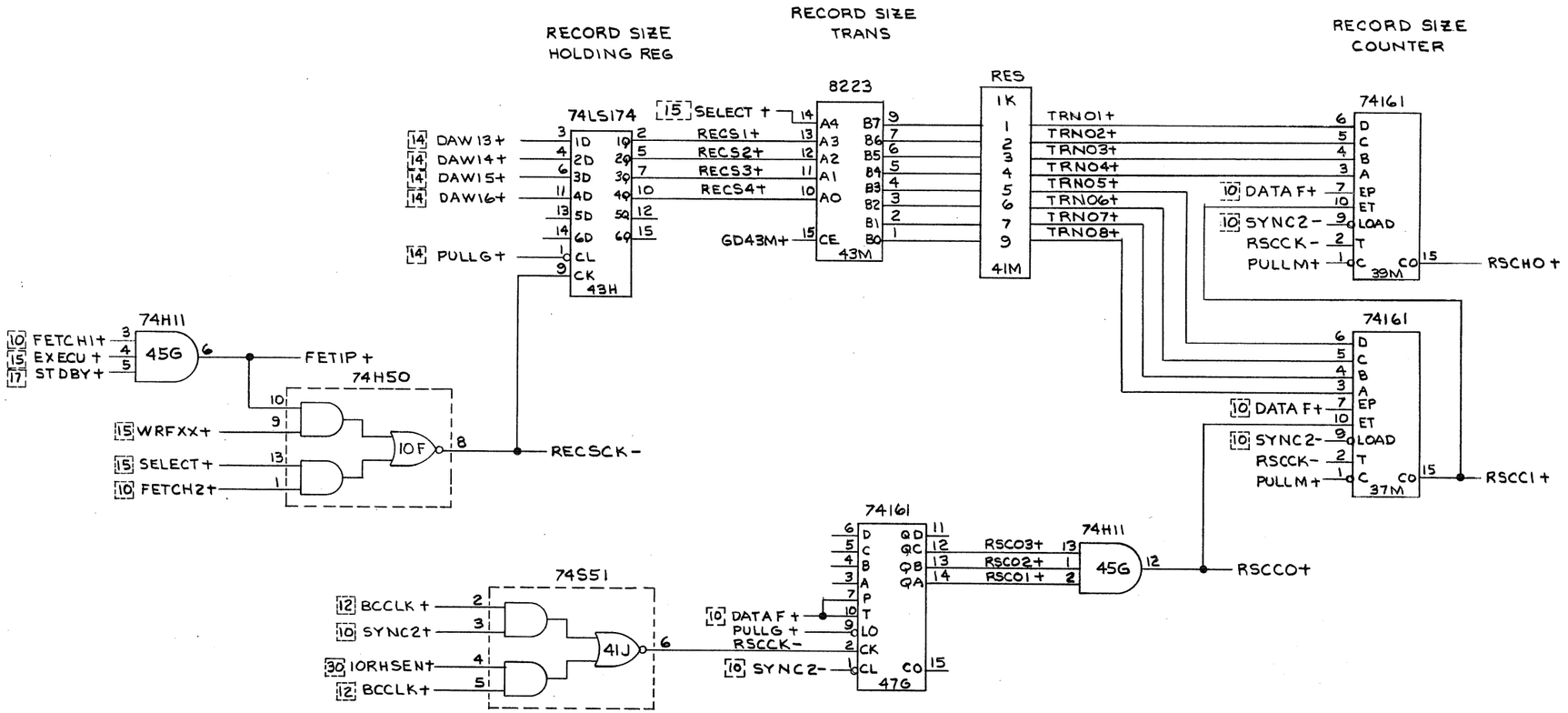




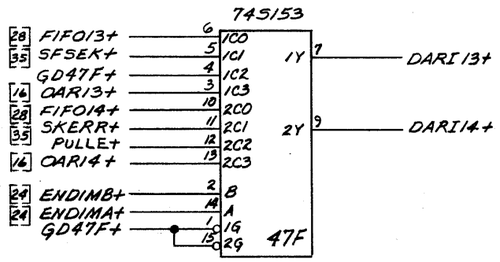
PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
WRITE REGISTER INPUT MUX	
SMC	4004
SHEET 19 OF	SIZE C
DWG. NO. LBD2437	REV. A

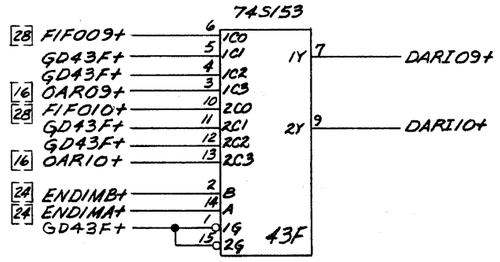


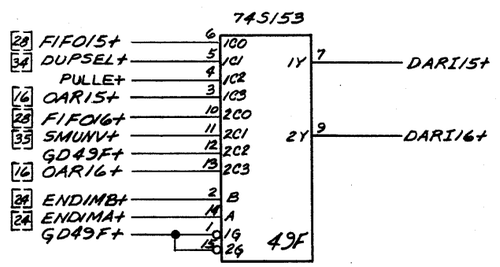
PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
DMA BUSY AND OVERUN	
SMC	4004
SHEET 20 OF	SIZE C · DWG. NO. LBD2437 · REV C

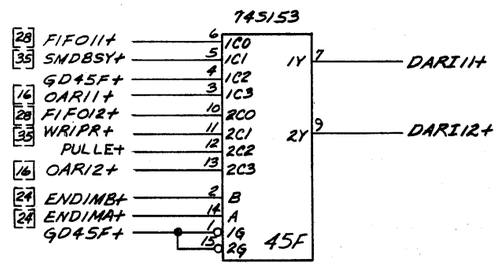


PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
RECORD SIZE COUNT			
SMC 4004			
SHEET 21 OF	SIZE C	DWG. NO. LBD 2437	REV. A



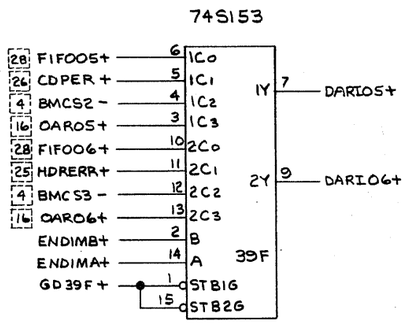


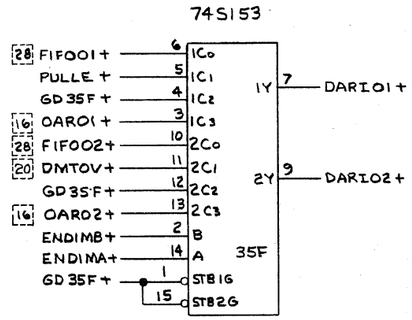


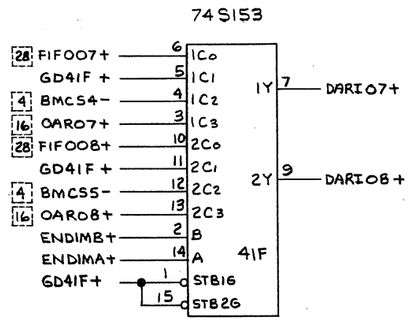


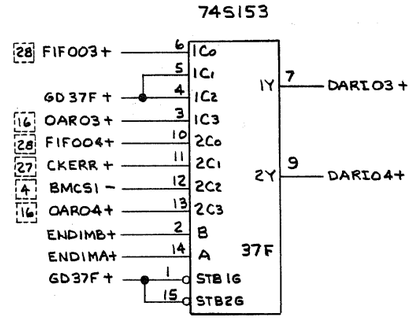
PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
DATA TO READ REG (RIGHT BYTE)	
SMC 4004	
SHEET 23 OF	SIZE C / DWG. NO. LBD2437 / REV. A

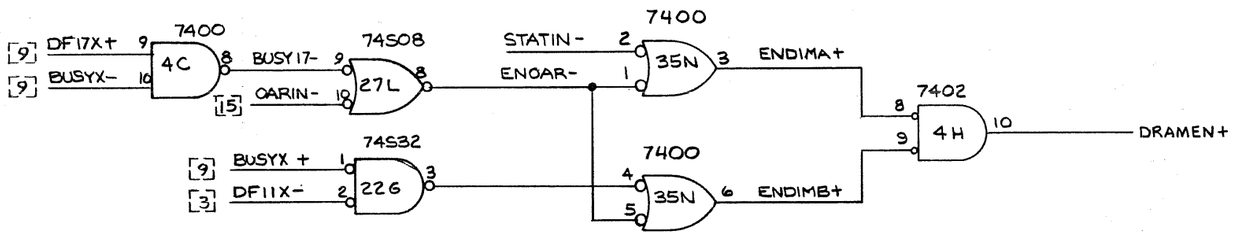
P0F-003





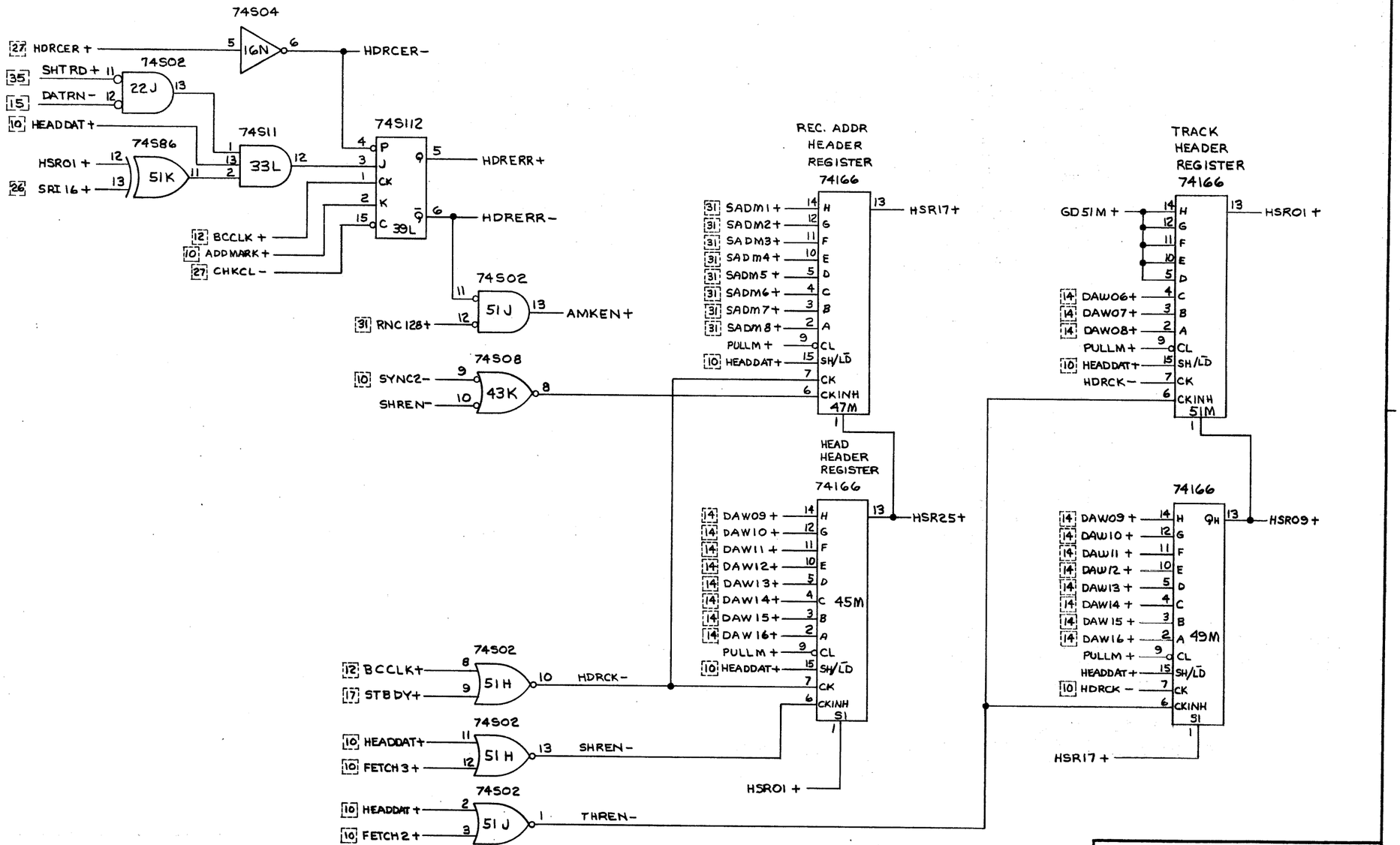






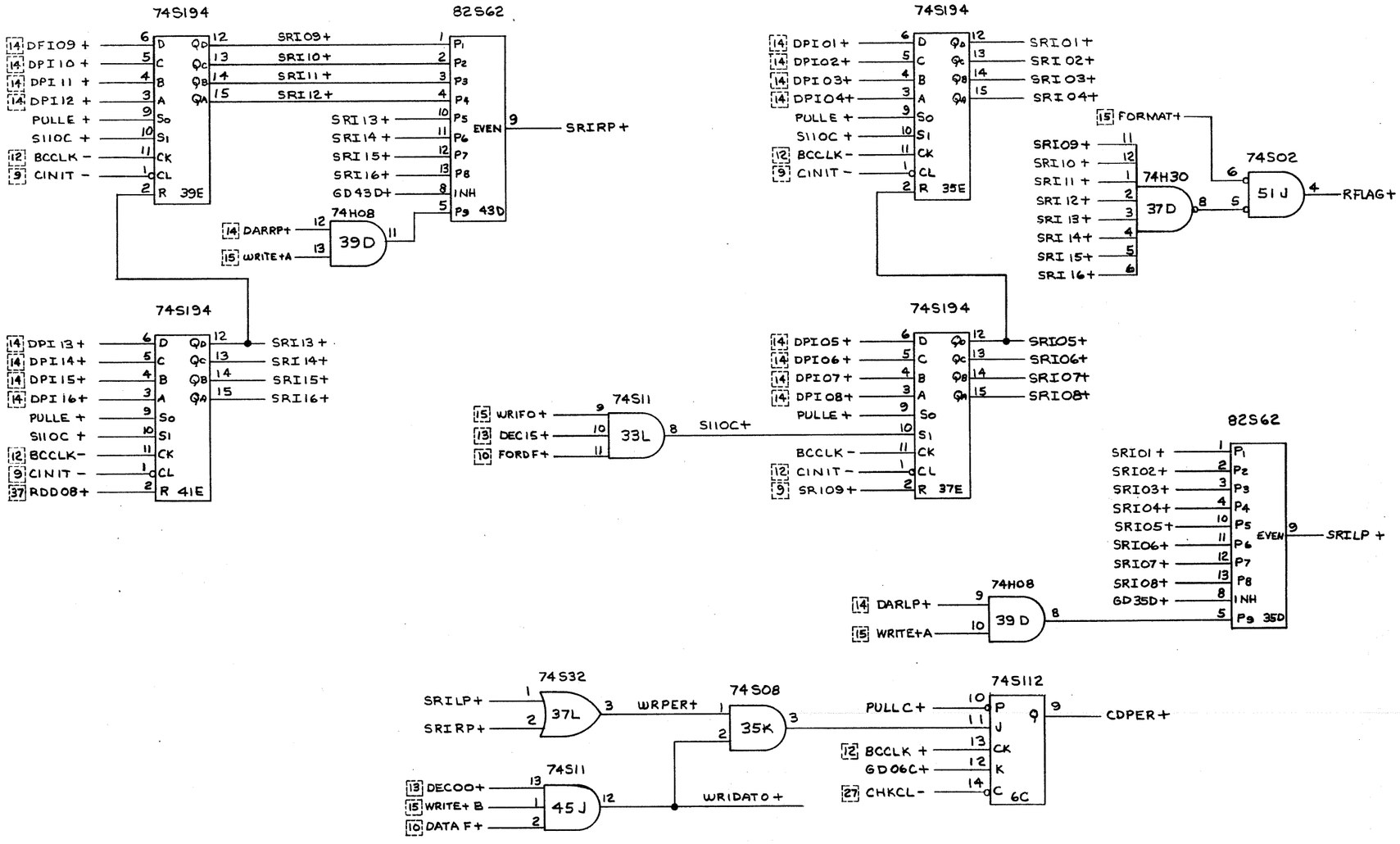
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DATA TO READ REG (LEFT BYTE)			
SMC 4004			
SHEET 24 OF	SIZE C	DWG. NO. LBD 2437	REV B

PDF-003

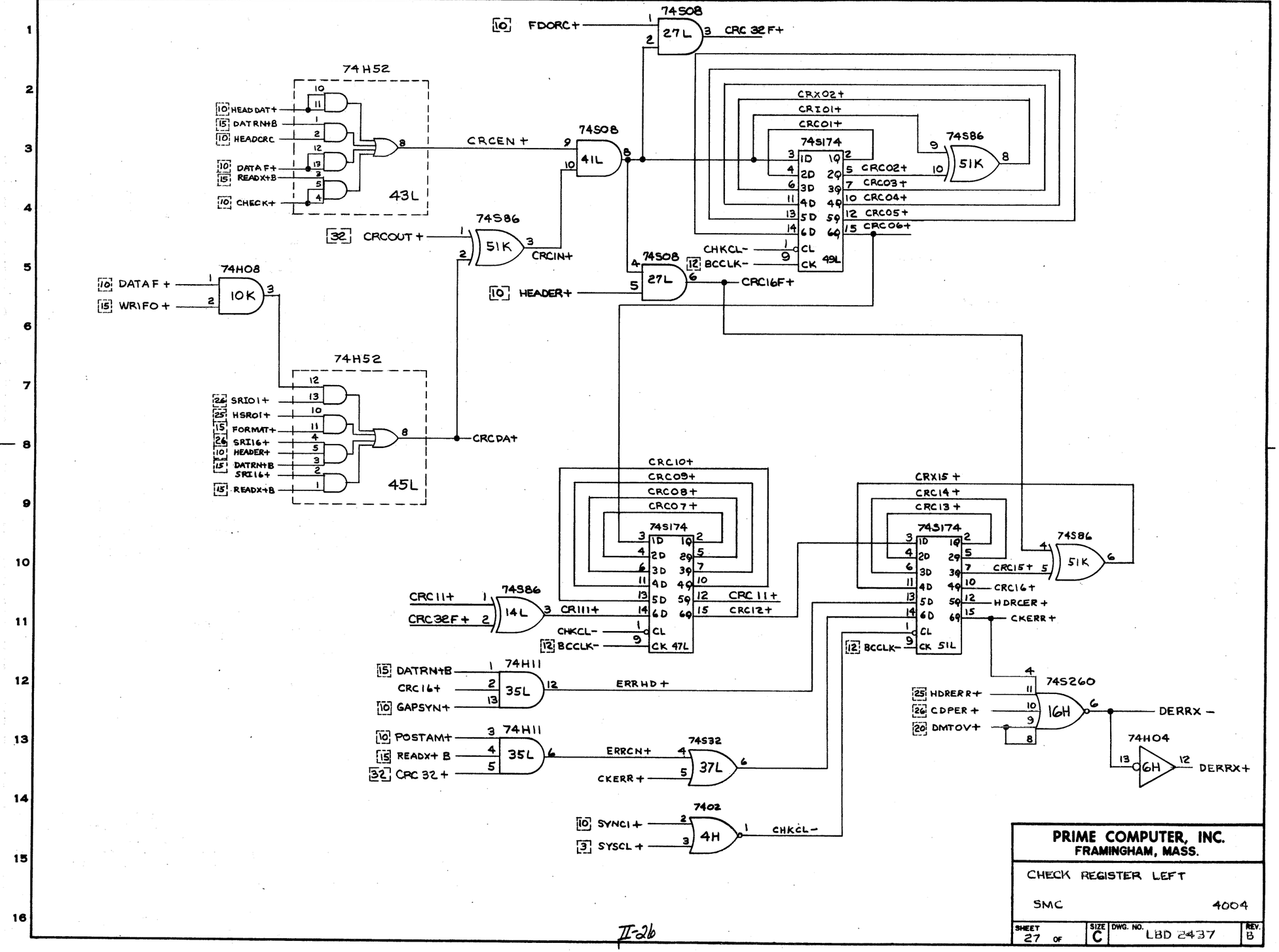


PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
HEADER REGISTER	
SMC	4004
SHEET 25 OF	SIZE C
DWG. NO. LBD 2437	REV. B

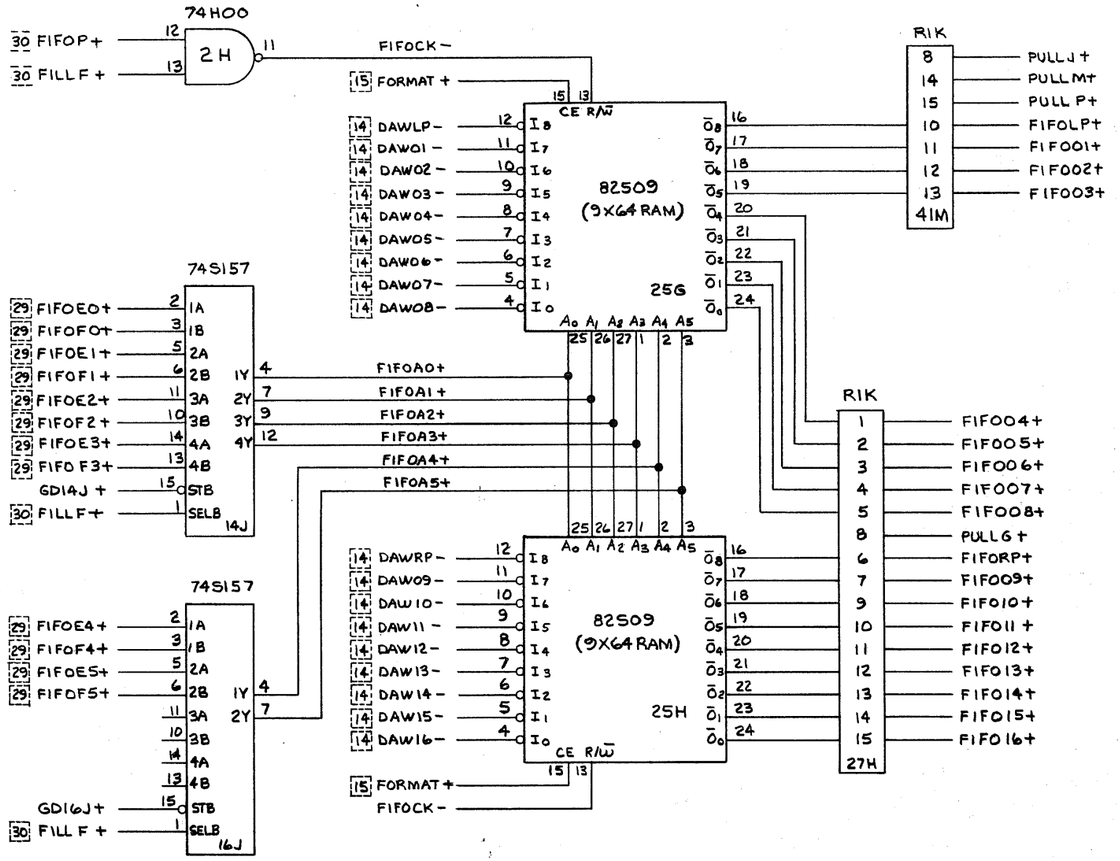
PDF-003



PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
I/O SHIFT REGISTER	
SMC	4004
SHEET 26 OF	SIZE C · DWG. NO. LBD2437 · REV. A



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
CHECK REGISTER LEFT			
SMC 4004			
SHEET 27 OF	SIZE C	DWG. NO. LBD 2437	REV. B



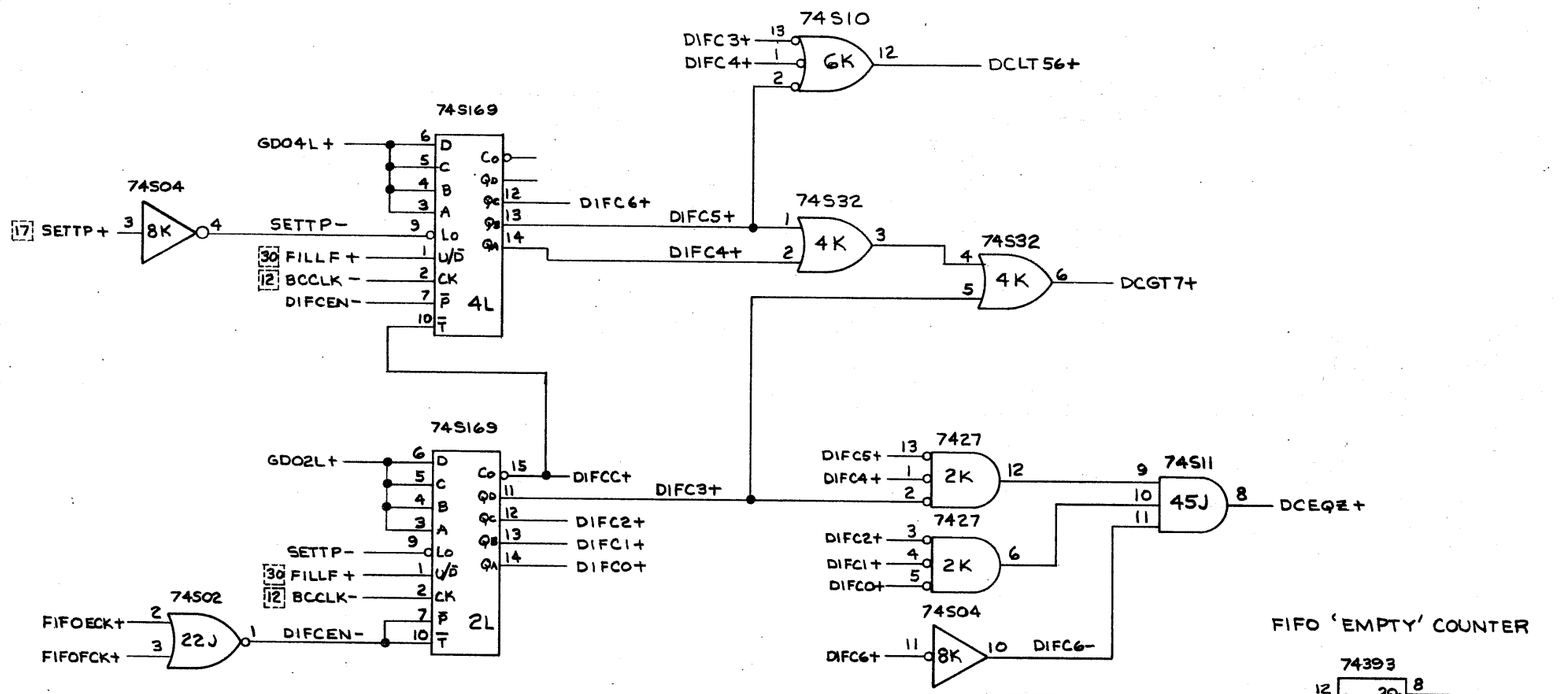
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

FIFO BUFFER

SMC 4004

SHEET 28 OF | SIZE C | DWG. NO. LBD2437 | REV. A

POF-003

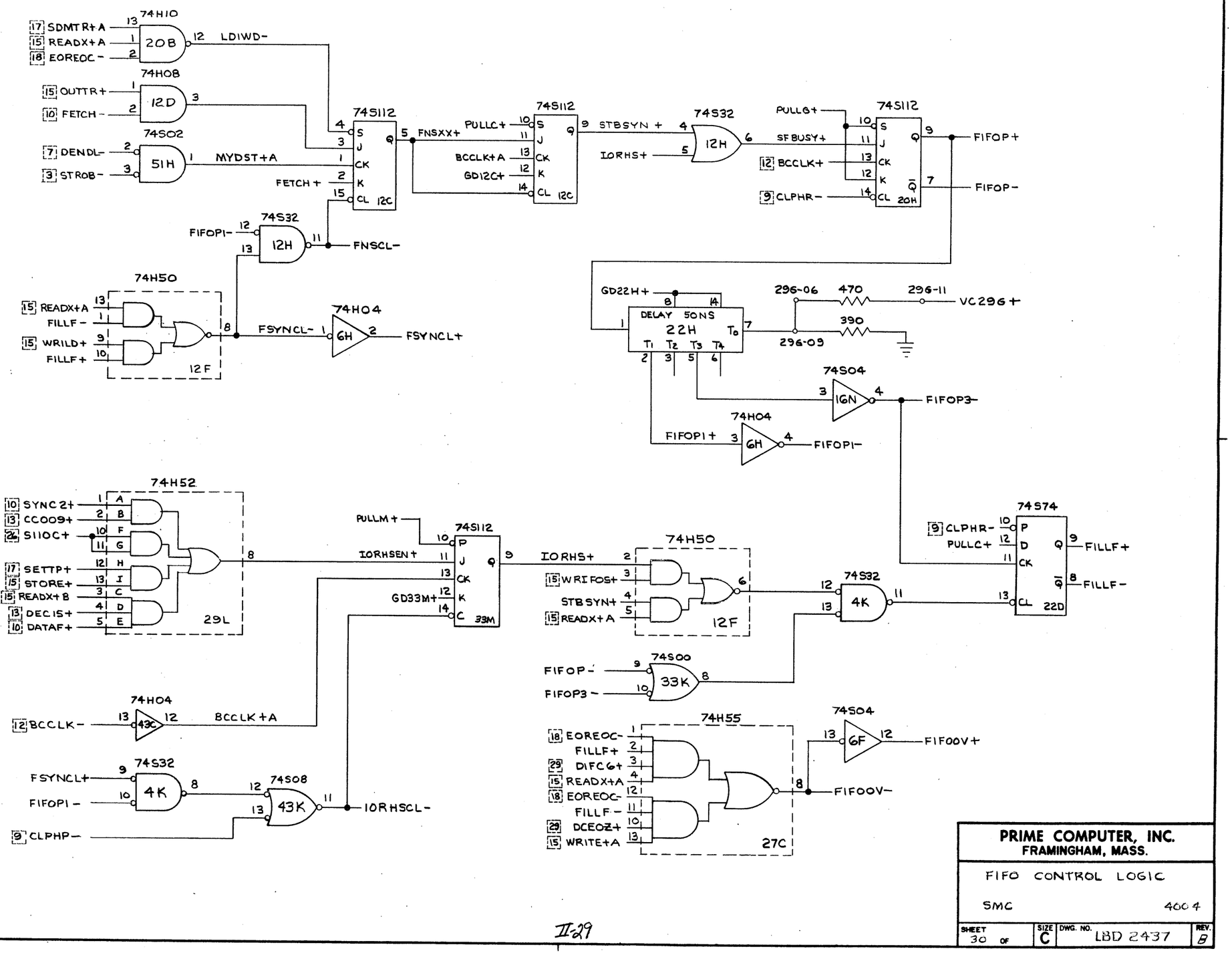


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

FIFO ADDRESS AND DIFFERENCE LOGIC

SMC 4004

SHEET 29 OF | SIZE C | DWG. NO. LBD 2437 | REV B



PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
FIFO CONTROL LOGIC	
SMC	4004
SHEET 30 OF	SIZE C
DWG. NO. LBD 2437	REV. B

RECORD ADDRESS REGISTER

74393

[9] CLPHR+ → 12 2CL
33J
13 2A
2QD 8 → RAD01+
2QC 9 → RAD02+
2QB 10 → RAD03+
2QA 11 → RAD04+

74393

[5] CLPHR+ → 2 1CL
33J
10 → 1A
1QD 6 → RAD05+
1QC 5 → RAD06+
1QB 4 → RAD07+
1QA 3 → RAD08+

74LS157

RAD01+ → 2 1A
[14] DAW01+ → 3 1B
RAD02+ → 5 2A
[14] DAW02+ → 6 2B
RAD03+ → 11 3A
[14] DAW03+ → 10 3B
RAD04+ → 14 4A
[14] DAW04+ → 13 4B
[15] DATRN+B → 1 SELB
GD35J+ → 15 G 35J

1Y 4 → SADM1+
2Y 7 → SADM2+
3Y 9 → SADM3+
4Y 12 → SADM4+

74LS157

RAD05+ → 2 1A
[14] DAW05+ → 3 1B
RAD06+ → 5 2A
[14] DAW06+ → 6 2B
RAD07+ → 11 3A
[14] DAW07+ → 10 3B
RAD08+ → 14 4A
[14] DAW08+ → 13 4B
[15] DATRN+B → 1 SELB
GD37J+ → 15 G 37J

1Y 4 → SADM5+
2Y 7 → SADM6+
3Y 9 → SADM7+
4Y 12 → SADM8+

RECORD NUMBER COUNTER

74H04

1 → 43G → 2 → RNCCO-

74161

[14] DAW01- → 6 D
[14] DAW02- → 5 C
[14] DAW03- → 4 B
[14] DAW04- → 3 A
[10] SETUP- → 9 Lo
[10] FETCH- → 1 CL
2 CK
10 T
7 P
29J

Co 15 → RNCCO+
QD 11 → RNC128+
QC 12
QB 13
QA 14

74161

[14] DAW05- → 6 D
[14] DAW06- → 5 C
[14] DAW07- → 4 B
[14] DAW08- → 3 A
[10] SETUP- → 9 Lo
[10] FETCH- → 1 CL
RNCCK- → 2 CK
PULLJ+ → 10 T
7 P
31J

Co 15 → RNCCX+
QD 11
QC 12
QB 13
QA 14

74H50

[10] ADDMARK+ → 3 10
[39] TAGEN+ → 13
[15] FORMAT+ → 1
27J
8 → RNCCK-

7474

PULLM+ → 4 S
2 D
3 CK
[35] INDEX+ → 1 C 35M
Q 5 → PULLM+
Q̄ 6

7474

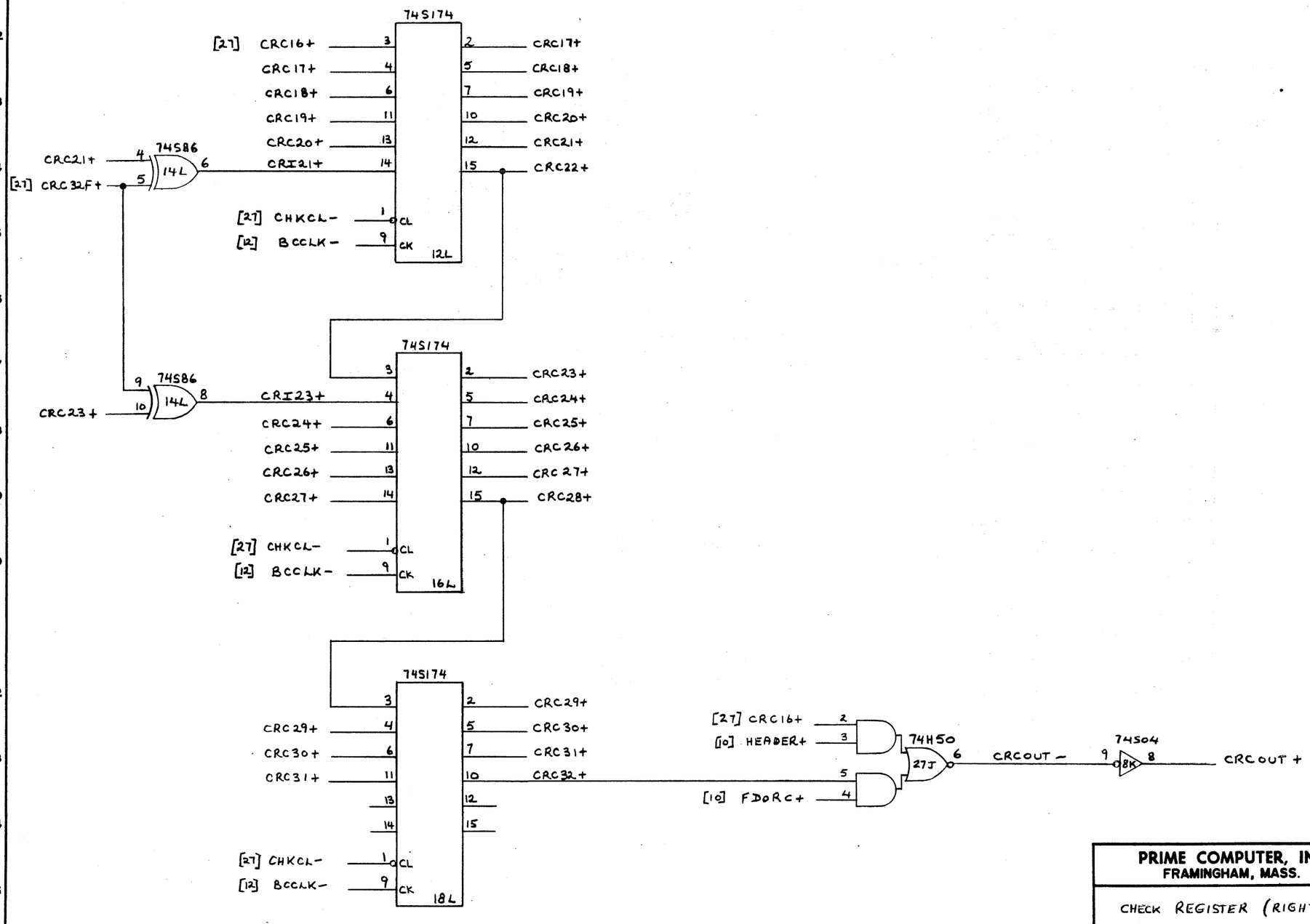
10 S
12 D
11 CK
13 C 35M
Q 9 → TWOIND+
Q̄ 8

74S112

PULLM+ → 4 S
3 J
1 CK
[12] BCCLK+ → 2 K
GD33M+ → 15 C 33M
[10] WAITX+
Q 5 → INDSYN+
Q̄ 6

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DOUBLE INDEX AND RECORD ADDRESS LOGIC			
SMC 4004			
SHEET 31 OF	SIZE C	DWG. NO. LBD2437	REV. A

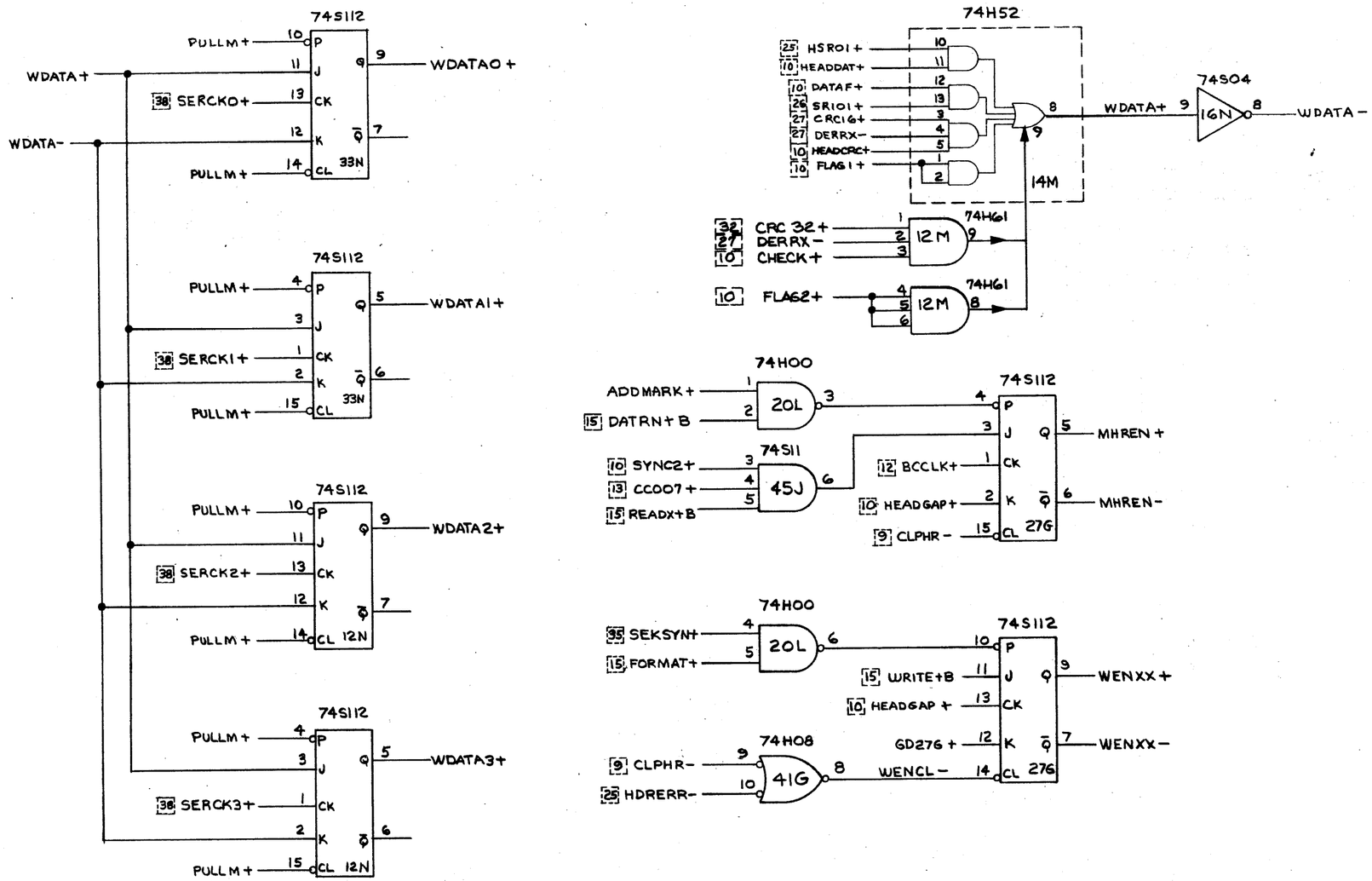
PDF-003



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

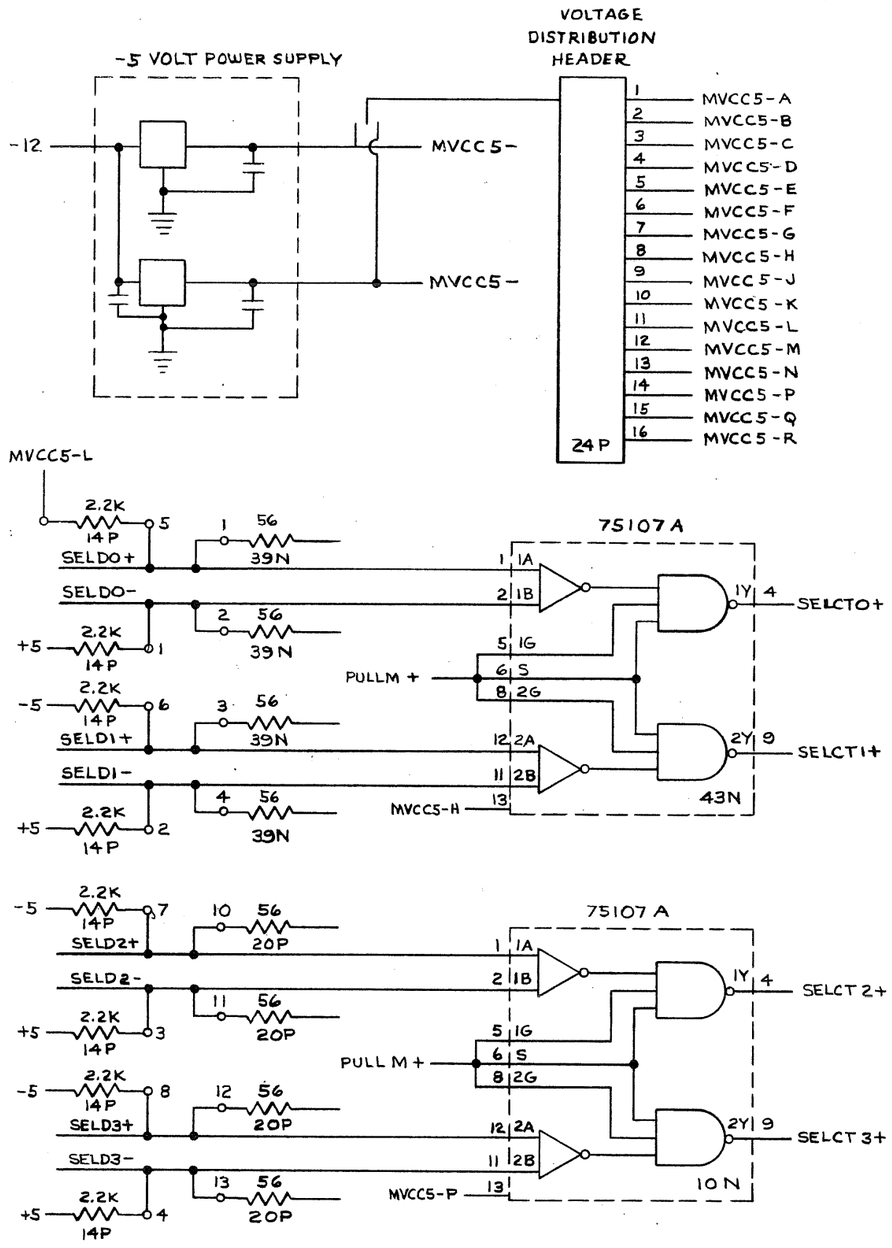
CHECK REGISTER (RIGHT)

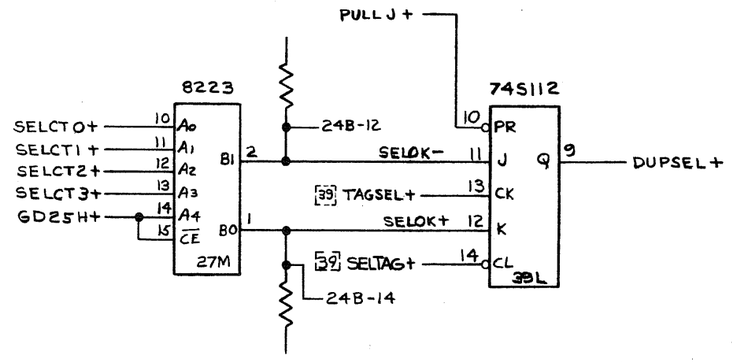
SHEET 32 OF 42 | SIZE C | DWG. NO. LBD 2437 | REV. B



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DATA CONTROL			
SMC 4004			
SHEET 33 OF	SIZE C	DWG. NO. LBD 2437	REV C

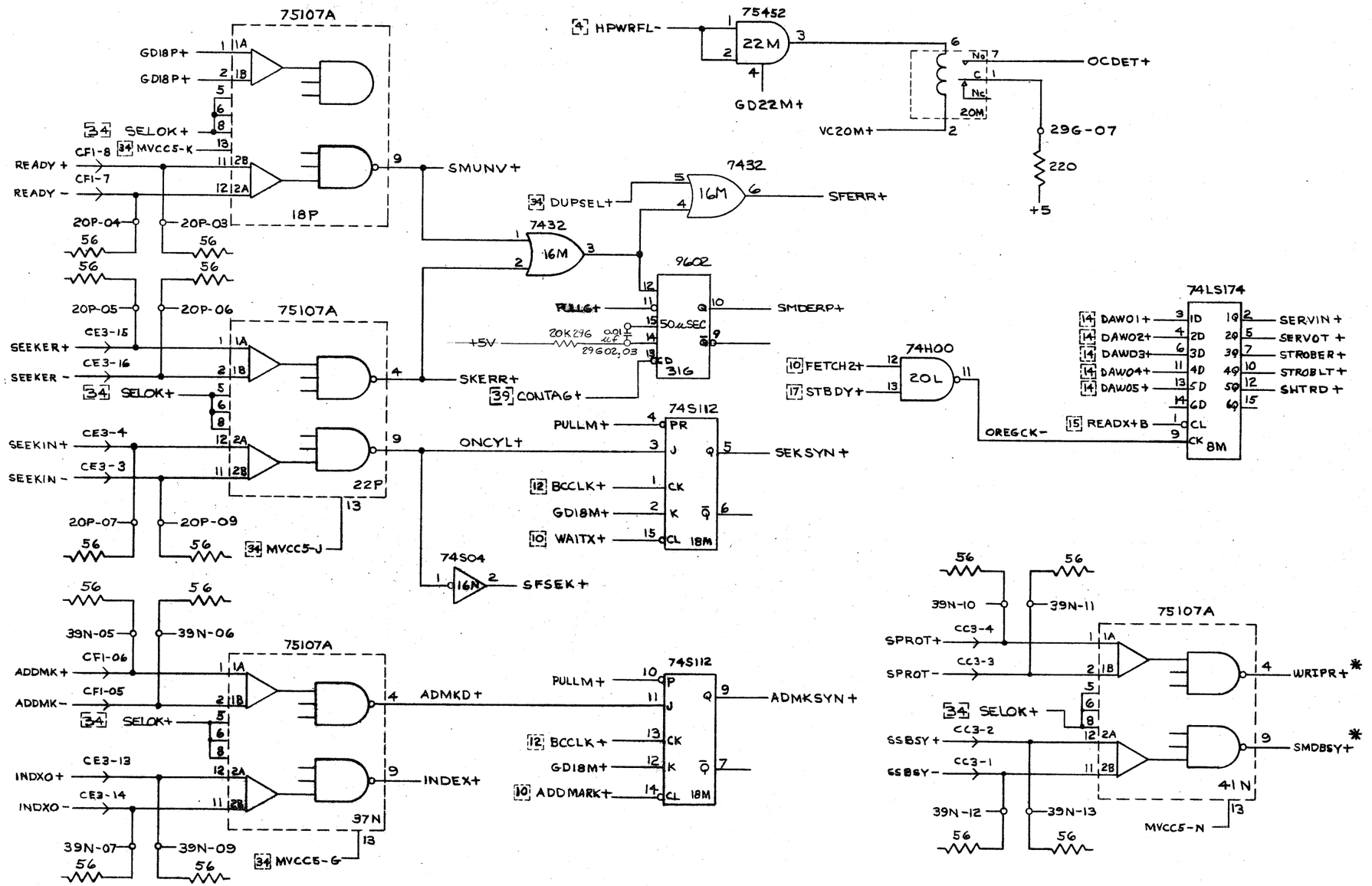
PDF-003





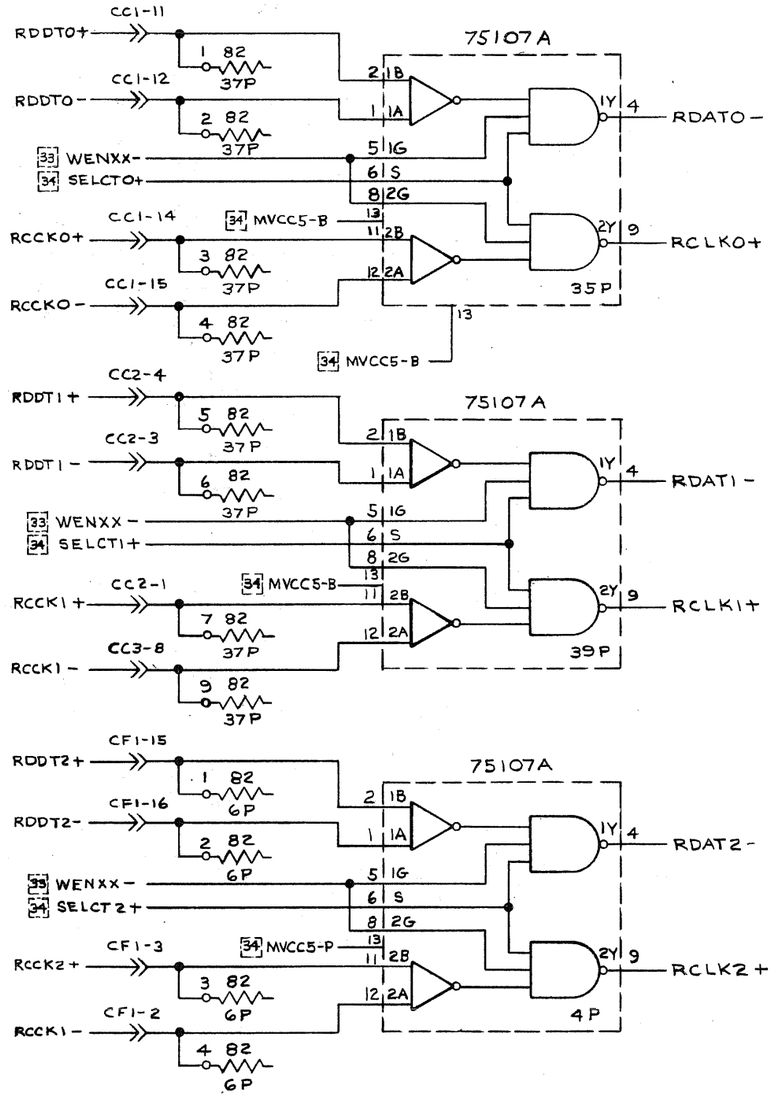
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DEVICE SELECT LOGIC			
SMC		-	4004
SHEET 34 OF	SIZE C	DWG. NO. LBD 2437	REV. B

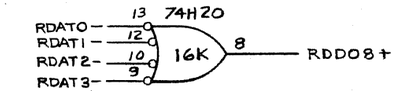
PDF-003

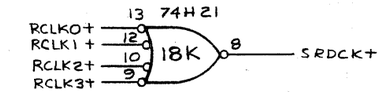


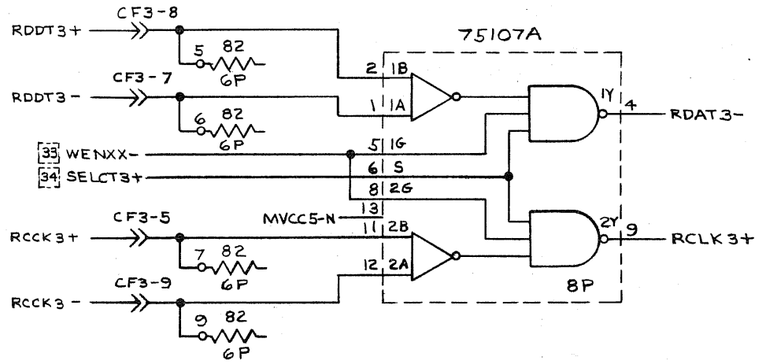
* GROUND FOR SINGLE PORT STYLE DEVICES.

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
MISC. SMD SIGNALS AND OFFSET			
SMC 4004			
SHEET 35 OF	SIZE C	DWG. NO. LBD 2437	REV. E







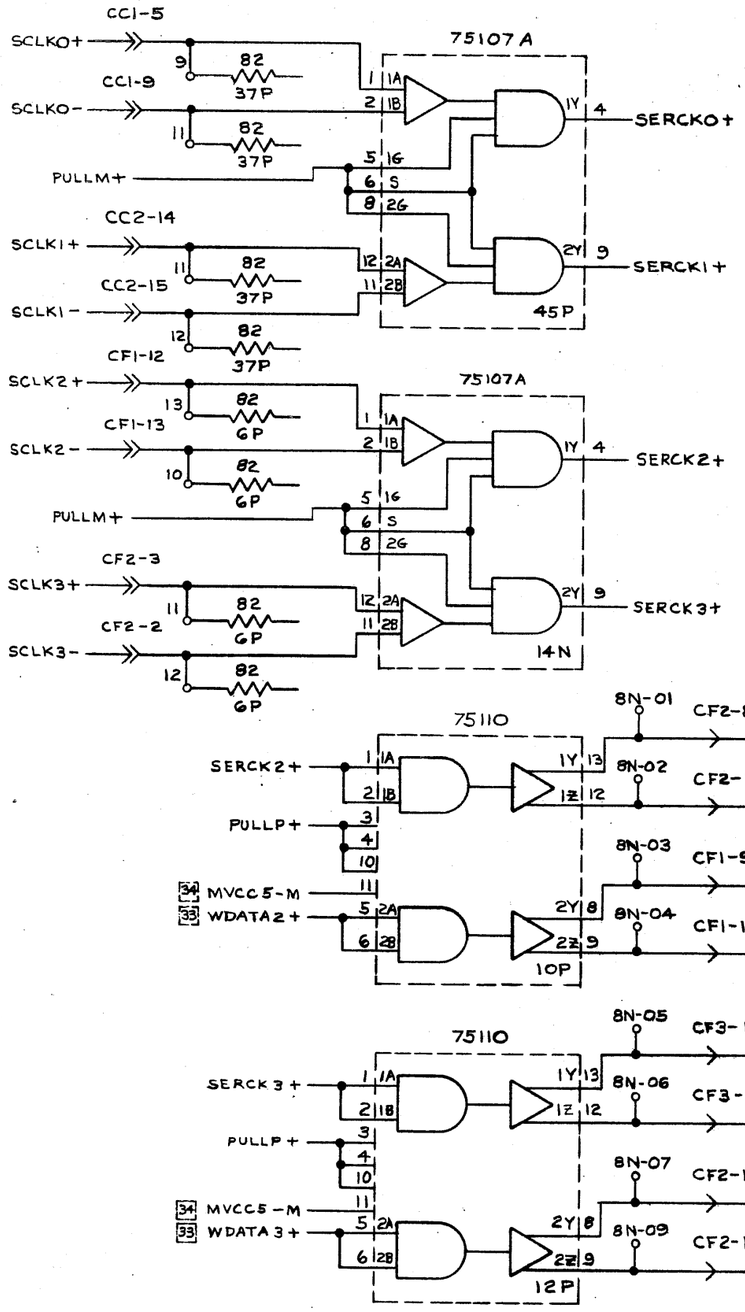


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

READ DATA AND CLOCK FROM SMD

SMC 4004

SHEET	SIZE	DWG. NO.	REV.
37 OF	C	LBD2437	A

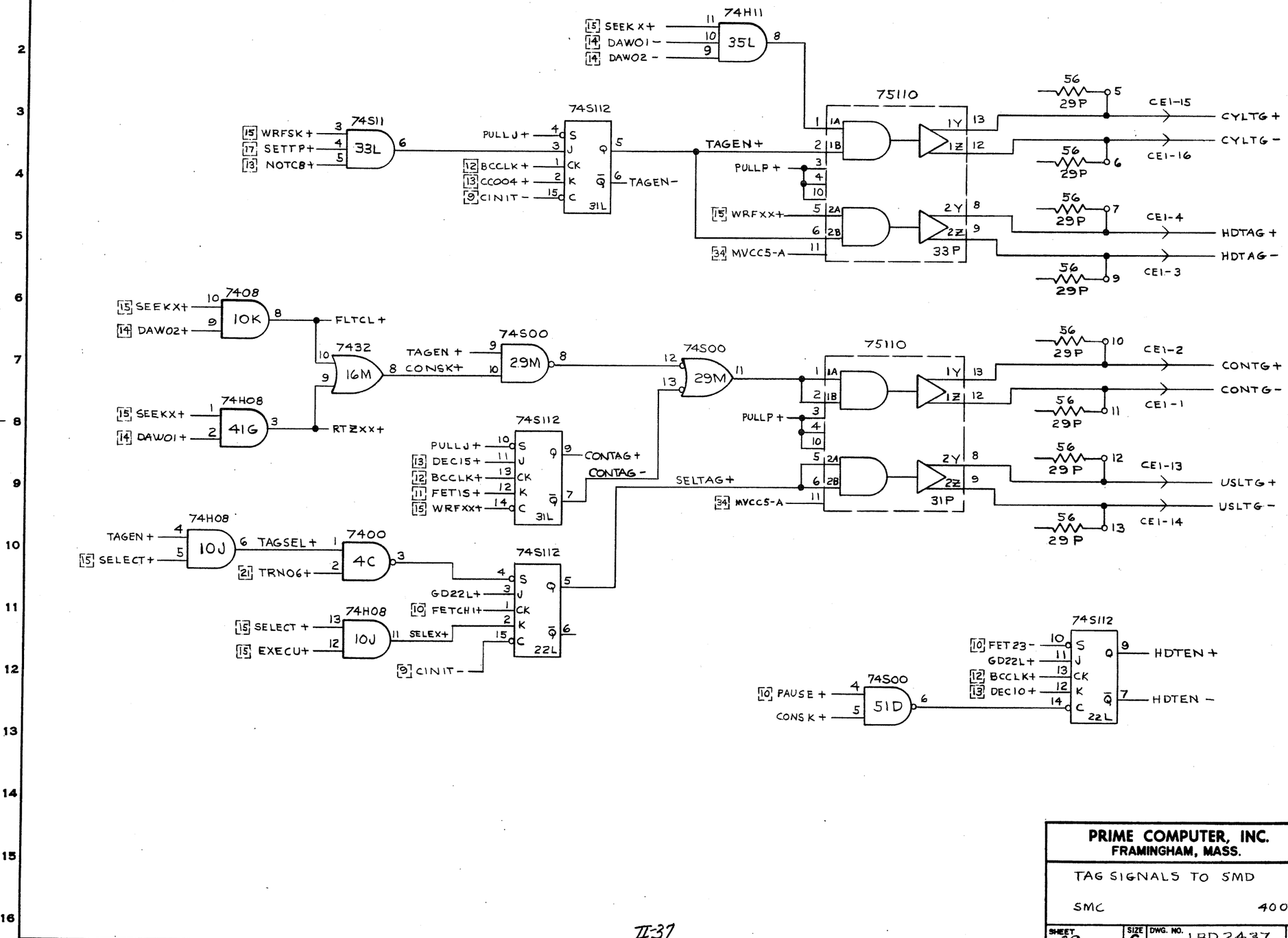


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

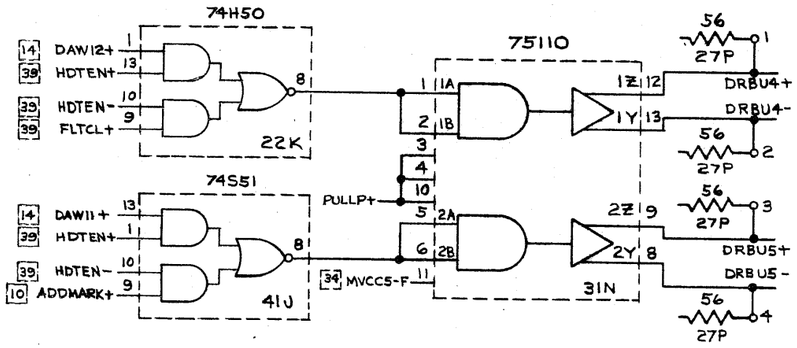
SERVO AND WRITE CLOCK

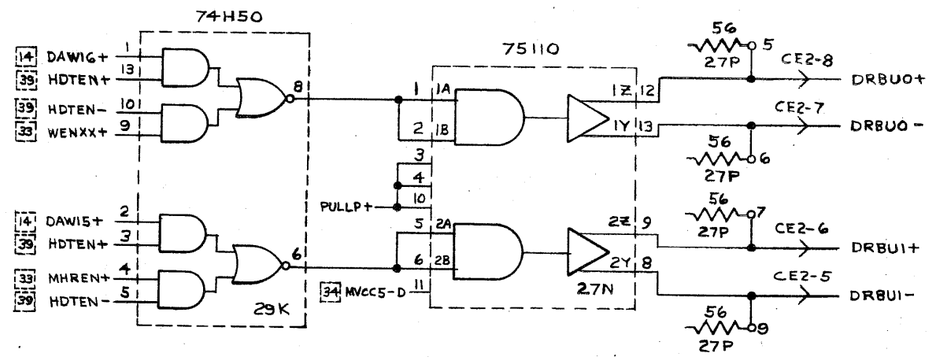
SMC 4004

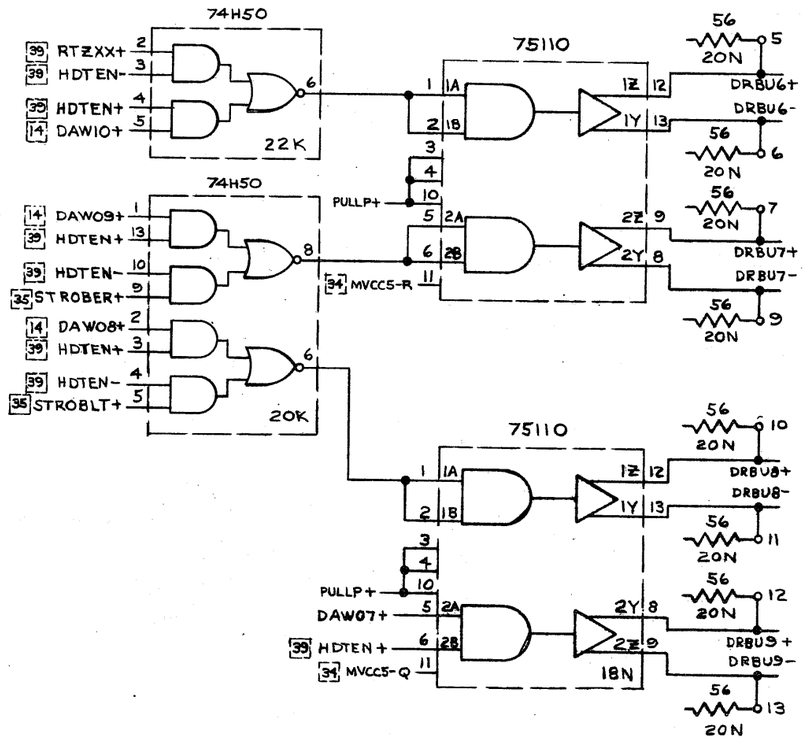
SHEET	SIZE	DWG. NO.	REV.
38 OF	C	LBD 2437	A

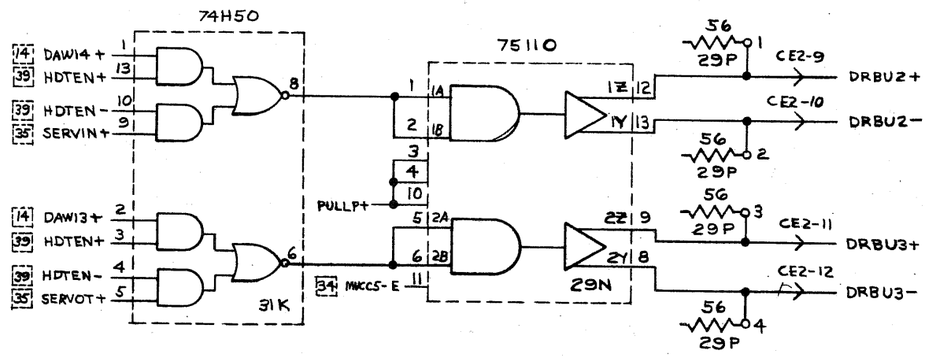


PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
TAG SIGNALS TO SMD			
SMC 4004			
SHEET 39 OF	SIZE C	DWG. NO. LBD 2437	REV C

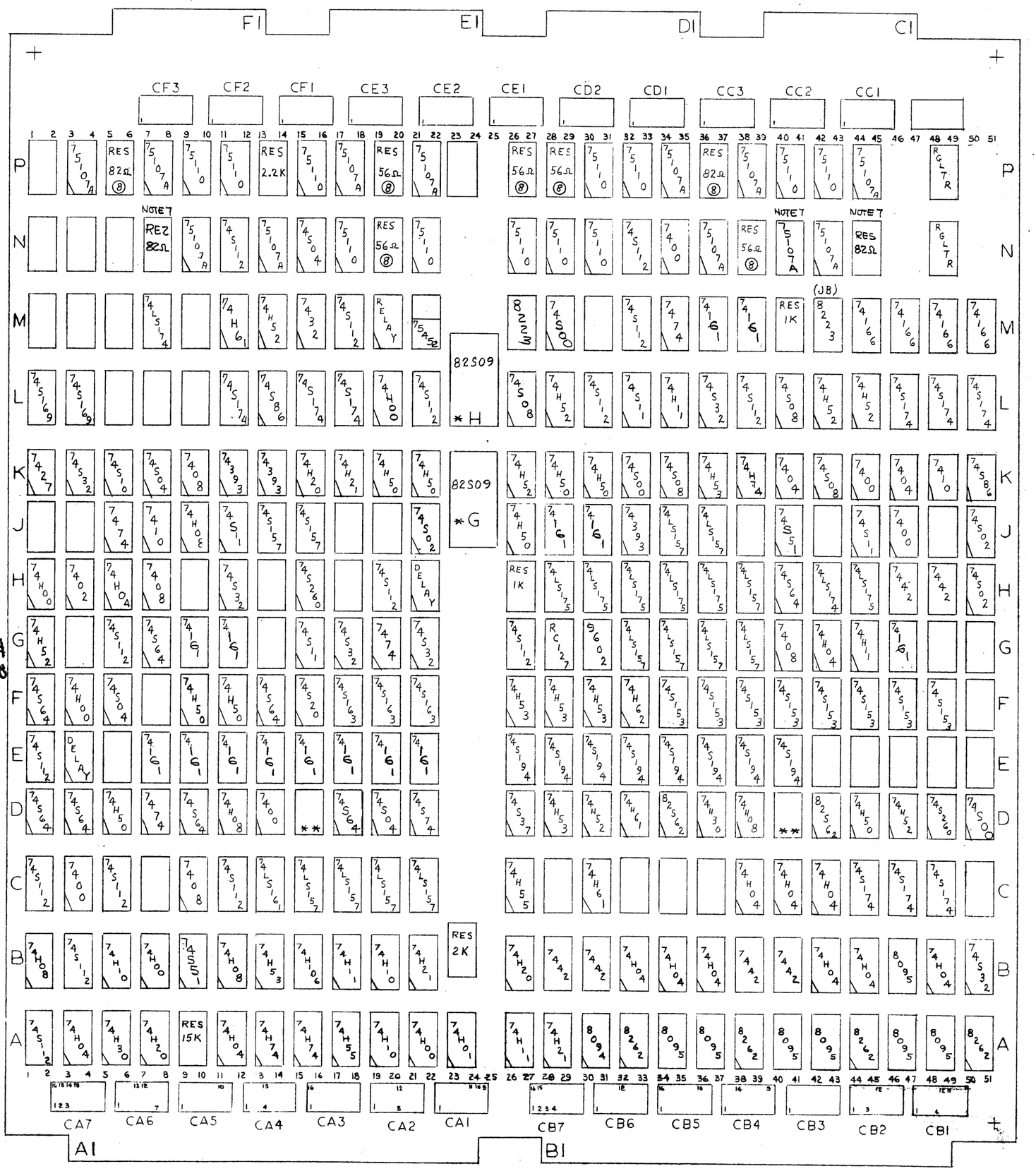








PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
BUS SIGNALS TO SMD			
SMC 4004			
SHEET 40 OF	SIZE C	DWG. NO. LBD2437	REV. A



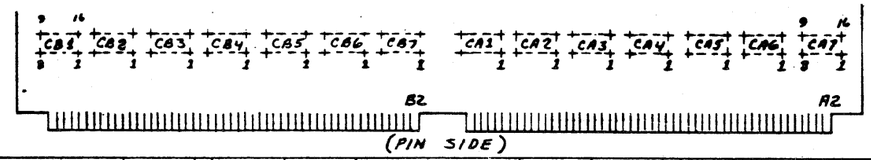
COMPONENT SIDE

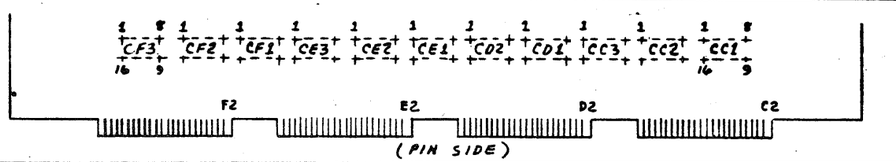
NOTES:

1. STANDARD I/O DIP SITES HAVE PROPER GND & VCC ETCH (ROW A & B)
2. ROW D & K HAVE GND & VCC ETCHED FOR 14 PIN DIPS (ie 7 IS GND & 14 IS VCC)
3. ALL OTHER ROWS (EXCEPT DIP SITES WITH *) HAVE GND & VCC ETCH FOR 16 PIN DIPS (ie 8 IS GND & 16 IS VCC)
4. ** MOUNTING HOLE AT DIP SITES 16 D & 41 D
5. PIN 1 IS LOCATED AT LOWER RIGHT
6. ⌞ = 14 PIN DIP
7. DUAL-PORT SMD ONLY
8. RESISTOR DIPS INDICATED WITH ⑧ ARE TO BE INSERTED IN BOARD WITH PIN 1 OF DIP IN PIN 9 OF SOCKET.

date 11/4/75	PRIME COMPUTER INC. NATICK, MASS.	
	DIP ALLOCATION STORAGE MODULE CONTROLLER SMC	
PCB 1769-001	SIZE C	DRWG NO. LBD2437 REV. C

LTR	DATE	REVISION	DR.	CK.





NAME	DIP SITE	CONN PIN
VCC1	CA7-15,16	CA-1
VCC1	CA7-15,16	CA-2
SHIELD(GND)	CA7-3	CA-3
BPCDCPN+	CA7-1	CA-4
BPCDEN +	CA7-8	CA-5
GND	CA7-2,3,14,13	CA-6
BPCDPNO -	CA7-12	CA-7
BPCDPNA -	CA7-4	CA-8
BPCDPNB -	CA7-10	CA-9
BPCDPNC -	CA7-5	CA-10
BPCDPND -	CA6-16	CA-11
BPCDPNE -	CA7-7	CA-12
BPCDPNF -	CA6-14	CA-13
BPCDPNG -	CA7-11	CA-14
BPCDPNH -	CA6-2	CA-15
BPCIEN +	CA7-9	CA-16
BPCIPNO -	CA6-4	CA-17
BPCIPNA -	CA6-15	CA-18
BPCIPNB -	CA6-6	CA-19
BPCIPNC -	CA6-3	CA-20
BPCIPND -	CA6-8	CA-21
SHIELD(GND)	CA6-5	CA-22
BPCICPN +	CA6-11	CA-23
GND	CA6-7,12,13	CA-24
BPCCHI +	CA6-9	CA-25
SHIELD(GND)	CA6-10	CA-26
	CA5-15	CA-27
	CA5-16	CA-28
	CA5-13	CA-29
BPCEOR +	CA5-14	CA-30
	CA5- 2	CA-31
	CA5-1	CA-32
	CA5-4	CA-33
	CA5-3	CA-34
	CA5-6	CA-35
	CA5-5	CA-36
	CA5-8	CA-37
BPCIOVI -	CA5-7	CA-38
	CA5-11	CA-39
	CA5-12	CA-40
	CA5-9	CA-41
GND	CA5-10	CA-42
BMCWDLR+	CA4-15	CA-43
	CA4-16	CA-44
	CA4-14	CA-45
	CA4-1	CA-46
BMCWDLL +	CA4-2	CA-47
SHIELD(GND)	CA4-3	CA-48
VCC1	CA4-4,13	CA-49
VCC1	CA4-4,13	CA-50

NAME	DIP SITE	CONN PIN
BMCADL +	CA4-6	CA-51
	CA4-5	CA-52
	CA4-8	CA-53
	CA4-7	CA-54
	CA4-11	CA-55
BMAPEL +	CA4-12	CA-56
BMAPER +	CA4-9	CA-57
BMDPEL -	CA4-10	CA-58
BMDPER -	CA3-15	CA-59
GND	CA3-16	CA-60
BMD01 +	CA3-13	CA-61
BMD02 +	CA3-1	CA-62
BMD03 +	CA3-2	CA-63
BMD04 +	CA3-3	CA-64
BMD05 +	CA3-4	CA-65
BMD06 +	CA3-5	CA-66
BMD07 +	CA3-6	CA-67
BMD08 +	CA3-7	CA-68
BMD09 +	CA3-8	CA-69
BMD10 +	CA3-12	CA-70
BMD11 +	CA3-11	CA-71
BMD12 +	CA3-10	CA-72
BMD13 +	CA3-9	CA-73
BMD14 +	CA2-16	CA-74
BMD15 +	CA2-15	CA-75
BMD16 +	CA2-1	CA-76
BMDLP -	CA2-13	CA-77
BMDRP -	CA2-3	CA-78
BMCSELC -	CA2-2	CA-79
GND	CA2-5,12	CA-80
BMCSELB -	CA2-4	CA-81
BMCSELV -	CA2-7	CA-82
BMCDINH -	CA2-6	CA-83
BMCWRB -	CA2-10	CA-84
BMCWLB -	CA2-8	CA-85
BMCRFSH -	CA1-16	CA-86
BMCEXS1 -	CA2-11	CA-87
BMCWSTRB -	CA1-14	CA-88
BMCEXS2 -	CA2-9	CA-89
BPCFCLK +	CA1-1	CA-90
BMCSS01 -	CA1-15	CA-91
BPCIRQ -	CA1-3	CA-92
BMCSS02 -	CA1-13	CA-93
BPCDRQ -	CA1-6	CA-94
BMCSS03 -	CA1-2	CA-95
BMCPRCH -	CA1-7	CA-96
BMCCNBL -	CA1-4	CA-97
GND	CA1-9,10,11	CA-98
VCC2	CA1-8	CA-99
VCC2	SPARE	CA-100

NAME	DIP SITE	CONN PIN
VCC1	CB7-1,2	CB-1
VCC1	CB7-1,2	CB-2
GND	CB7-3,4,5,16	CB-3
TSO[SPARE]	CB7-5	CB-4
BMA99 -	CB7-8	CB-5
BMA00 -	CB7-7	CB-6
BMA01 -	CB7-12	CB-7
BMA02 -	CB7-13	CB-8
BMA03 -	CB7-10	CB-9
BMA04 -	CB7-11	CB-10
BMA05 -	CB6-16	CB-11
BMA06 -	CB7-9	CB-12
BMA07 -	CB6-14	CB-13
BMA08 -	CB6-15	CB-14
BMA09 -	CB6-2	CB-15
BMA10 -	CB6-1	CB-16
BMA11 -	CB6-4	CB-17
BMA12 -	CB6-3	CB-18
BMA13 -	CB6-6	CB-19
BMA14 -	CB6-5	CB-20
BMA15 -	CB6-8	CB-21
BMA16 -	CB6-7	CB-22
BMALP -	CB6-11	CB-23
BMARP -	CB6-13	CB-24
HPWRFL -	CB6-9	CB-25
GND	CB6-12	CB-26
VCORE1	CB5-15	CB-27
VCORE1	CB6-10	CB-28
BPA01 +	CB5-13	CB-29
GND	CB5-16	CB-30
BPA02 +	CB5-2	CB-31
BPA03 +	CB5-1	CB-32
BPA04 +	CB5-4	CB-33
BPA05 +	CB5-3	CB-34
BPA06 +	CB5-6	CB-35
BPA07 +	CB5-5	CB-36
BPA08 +	CB5-8	CB-37
BPA09 +	CB5-7	CB-38
BPA10 +	CB5-11	CB-39
BPA11 +	CB5-14	CB-40
HSYSCLR -	CB5-9	CB-41
GND	CB5-10	CB-42
VCORE2	CB4-15	CB-43
VCORE2	CB4-16	CB-44
BPDPEL -	CB4-13	CB-45
GND	CB4-1,14	CB-46
BPDPER -	CB4-2	CB-47
BPAPEL -	CB4-3	CB-48
BPA99 +	CB4-4	CB-49
BPA00 +	CB4-5	CB-50

NAME	DIP SITE	CONN PIN
BPA12 +	CB4-6	CB-51
BPA13 +	CB4-7	CB-52
BPA14 +	CB4-8	CB-53
BPA15 +	CB4-12	CB-54
BPA16 +	CB4-11	CB-55
BPALP +	CB4-10	CB-56
GND	CB4-9	CB-57
BPARP +	CB3-16	CB-58
BPCPIO +	CB3-15	CB-59
BPAPER -	CB3-14	CB-60
BPC60CY +	CB3-13	CB-61
BPCREDY -	CB3-1	CB-62
BPDLP +	CB3-2	CB-63
	CB3-3	CB-64
BPD01 +	CB3-4	CB-65
BPDRP +	CB3-5	CB-66
BPD02 +	CB3-6	CB-67
BPD03 +	CB3-7	CB-68
BPD04 +	CB3-8	CB-69
BPD05 +	CB3-12	CB-70
BPD06 +	CB3-11	CB-71
BPD07 +	CB3-10	CB-72
BPD08 +	CB3-9	CB-73
BPD09 +	CB2-16	CB-74
BPD10 +	CB2-15	CB-75
BPD11 +	CB2-14	CB-76
V12 -	CB2-13	CB-77
V12 -	CB2-1	CB-78
BPD12 +	CB2-2	CB-79
GND	CB2-3,12	CB-80
BPD13 +	CB2-4	CB-81
BPD14 +	CB2-5	CB-82
BPD15 +	CB2-6	CB-83
BPD16 +	CB2-7	CB-84
BPCMOD0 +	CB2-8	CB-85
BPCMOD1 +	CB2-10	CB-86
BPCMOD2 +	CB2-11	CB-87
BPCMOD3 +	CB1-16	CB-88
BPCINMD +	CB2-9	CB-89
BPCSCLK +	CB1-14	CB-90
V12 +	CB1-15	CB-91
V12 +	NOT USED	CB-92
HRUN -	CB1-13	CB-93
HRUN -	CB1-3	CB-94
BPCSTRB +	CB1-2	CB-95
GND	CB1-4,11,12	CB-96
VSS	CB1-5	CB-97
VSS	NOT USED	CB-98
VBB	CB1-6	CB-99
VBB	NOT USED	CB-100

NAME	DIP SITE	CONN PIN
WDAT0 +	CC1-8	CC-1
WDAT0 -	CC1-7	CC-2
GD41P+A	CC1-6	CC-3
SCLK0 +	CC1-5	CC-4
SCLK0 -	CC1-9	CC-5
GD45P+A	CC1-10	CC-6
RDDT0 +	CC1-11	CC-7
RDDT0 -	CC1-12	CC-8
GD35P+A	CC1-13	CC-9
RCCK0 +	CC1-14	CC-10
RCCK0 -	CC1-15	CC-11
GD35P+B	CC1-12	CC-12
WCLK0 +	CC1-4	CC-13
WCLK0 -	CC1-3	CC-14
GD41P+B	CC1-2	CC-15
	CC1-1	CC-16
	CC2-8	CC-17
	CC2-7	CC-18
	CC2-6	CC-19
SELD0 +	CC2-5	CC-20
SELD0 -	CC2-9	CC-21
	CC2-10	CC-22
WDAT1 +	CC2-11	CC-23
WDAT1 -	CC2-12	CC-24
GD43P+A	CC2-13	CC-25
SCLK1 +	CC2-14	CC-26
SCLK1 -	CC2-15	CC-27
GD45P+B	CC2-16	CC-28
RDDT1 +	CC2-4	CC-29
RDDT1 -	CC2-3	CC-30
GD39P+A	CC2-2	CC-31
RCCK1 +	CC2-1	CC-32
RCCK1 -	CC3-8	CC-33
GD39P+B	CC3-7	CC-34
WCLK1 +	CC3-6	CC-35
WCLK1 -	CC3-5	CC-36
GD43P+B	CC3-9	CC-37
	CC3-10	CC-38
	CC3-11	CC-39
	CC3-12	CC-40
	CC3-13	CC-41
SELD1 +	CC3-14	CC-42
SELD1 -	CC3-15	CC-43
	CC3-16	CC-44

B CABLE TO SMD NO'S 1 AND 2

NAME	DIP SITE	CONN PIN
SPROT +	CC3-4	CD-1
SPROT -	CC3-3	CD-2
SSBSY +	CC3-2	CD-3
SSBSY -	CC3-1	CD-4
	CD1-8	CD-5
	CD1-7	CD-6
	CD1-6	CD-7
	CD1-5	CD-8
	CD1-9	CD-9
	CD1-10	CD-10
	CD1-11	CD-11
	CD1-12	CD-12
	CD1-13	CD-13
	CD1-14	CD-14
	CD1-15	CD-15
	CD1-16	CD-16
	CD1-4	CD-17
	CD1-3	CD-18
	CD1-2	CD-19
	CD1-1	CD-20
	CD2-8	CD-21
	CD2-7	CD-22
	CD2-6	CD-23
	CD2-5	CD-24
	CD2-9	CD-25
	CD2-10	CD-26
	CD2-11	CD-27
	CD2-12	CD-28
	CD2-13	CD-29
	CD2-14	CD-30
	CD2-15	CD-31
	CD2-16	CD-32
	CD2-4	CD-33
	CD2-3	CD-34
	CD2-2	CD-35
	CD2-1	CD-36
	CE1-8	CD-37
	CE1-7	CD-38
	CE1-6	CD-39
	CE1-5	CD-40
	CE1-9	CD-41
	CE1-10	CD-42
	CE1-11	CD-43
	CE1-12	CD-44

A CABLE TO SMD

NAME	DIP SITE	CONN PIN
USLTG +	CE1-13	CE-1
USLTG -	CE1-14	CE-2
CYLTG +	CE1-15	CE-3
CYLTG -	CE1-16	CE-4
HDTAG +	CE1-4	CE-5
HDTAG -	CE1-3	CE-6
CONTG +	CE1-2	CE-7
CONTG -	CE1-1	CE-8
DRBU0 +	CE2-8	CE-9
DRBU0 -	CE2-7	CE-10
DRBU1 +	CE2-6	CE-11
DRBU1 -	CE2-5	CE-12
DRBU2 +	CE2-9	CE-13
DRBU2 -	CE2-10	CE-14
DRBU3 +	CE2-11	CE-15
DRBU3 -	CE2-12	CE-16
DRBU4 +	CE2-13	CE-17
DRBU4 -	CE2-14	CE-18
DRBU5 +	CE2-15	CE-19
DRBU5 -	CE2-16	CE-20
DRBU6 +	CE2-4	CE-21
DRBU6 -	CE2-3	CE-22
DRBU7 +	CE2-2	CE-23
DRBU7 -	CE2-1	CE-24
DRBU8 +	CE3-8	CE-25
DRBU8 -	CE3-7	CE-26
DRBU9 +	CE3-6	CE-27
DRBU9 -	CE3-5	CE-28
USL20 +	CE3-9	CE-29
USL20 -	CE3-10	CE-30
USL21 +	CE3-11	CE-31
USL21 -	CE3-12	CE-32
INDX0 +	CE3-13	CE-33
INDX0 -	CE3-14	CE-34
SEEKER +	CE3-15	CE-35
SEEKER -	CE3-16	CE-36
SEEKIN +	CE3-4	CE-37
SEEKIN -	CE3-3	CE-38
OCDET +	CE3-2	CE-39
GD20P +	CE3-1	CE-40
READY +	CF1-8	CE-41
READY -	CF1-7	CE-42
ADDMK +	CF1-6	CE-43
ADDMK -	CF1-5	CE-44

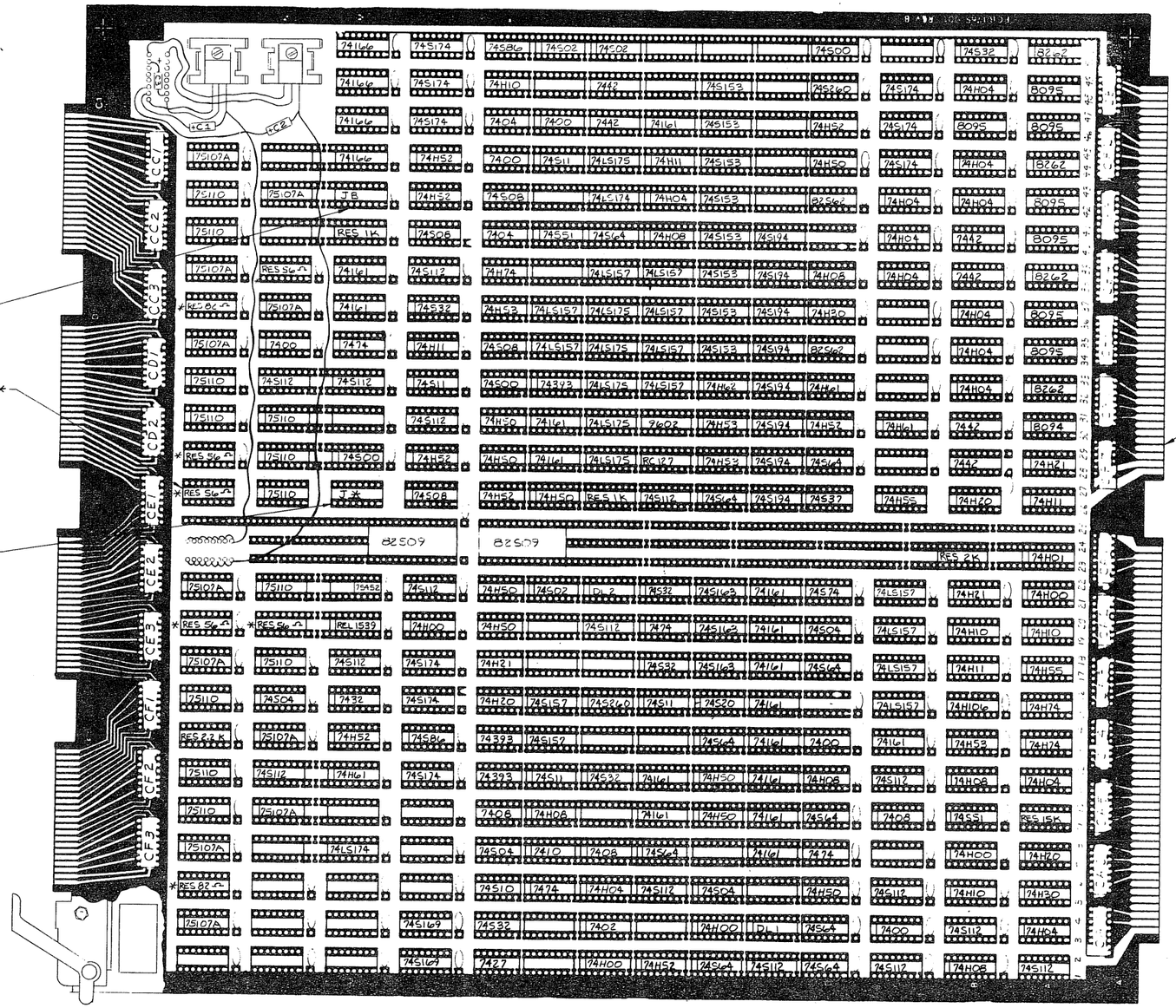
B CABLE TO SMD NO'S 3 AND 4

NAME	DIP SITE	CONN PIN
WDAT2 +	CF1-9	CF-1
WDAT2 -	CF1-10	CF-2
GD10P+A	CF1-11	CF-3
SCLK2 +	CF1-12	CF-4
SCLK2 -	CF1-13	CF-5
GD14N+A	CF1-14	CF-6
RDDT2 +	CF1-15	CF-7
RDDT2 -	CF1-16	CF-8
GD04P+A	CF1-4	CF-9
RCCK2 +	CF1-3	CF-10
RCCK2 -	CF1-2	CF-11
GD04P+B	CF1-1	CF-12
WCLK2 +	CF2-8	CF-13
WCLK2 -	CF2-7	CF-14
GD10P+B	CF2-6	CF-15
	CF2-5	CF-16
	CF2-9	CF-17
	CF2-10	CF-18
	CF2-11	CF-19
SELD2 +	CF2-12	CF-20
SELD2 -	CF2-13	CF-21
	CF2-14	CF-22
WDAT3 +	CF2-15	CF-23
WDAT3 -	CF2-16	CF-24
GD12P+A	CF3-4	CF-25
SCLK3 +	CF3-5	CF-26
SCLK3 -	CF3-2	CF-27
GD14N+B	CF2-1	CF-28
RDDT3 +	CF3-8	CF-29
RDDT3 -	CF3-7	CF-30
GD08P+A	CF3-6	CF-31
RCCK3 +	CF3-5	CF-32
RCCK3 -	CF3-9	CF-33
GD08P+B	CF3-10	CF-34
WCLK3 +	CF3-11	CF-35
WCLK3 -	CF3-12	CF-36
GD12P+B	CF3-13	CF-37
	CF3-14	CF-38
	CF3-15	CF-39
	CF3-16	CF-40
	CF3-4	CF-41
SELD3 +	CF3-3	CF-42
SELD3 -	CF3-2	CF-43
	CF3-1	CF-44

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	CONNECTOR SIGNAL NAME LIST, STORAGE MODULE CONTROLLER
	APPRD	
	USED ON	SCALE / SIZE C / DWG. NO. LBD2437 / REV. A
	NEXT ASSY	SHEET 42 OF

TE40

M	LTR	DATE	REVISION	DR.	CK.
	J	3-31-76	PER ECR 2028	JJT	SWD
	K	1-4-77	PER ECR 2012	JJT	SWD
	L	3-9-77	REVISED PER ECR 2113	JJT	SWD
	M	4-11-77	REVISED PER ECR 2158	JJT	SWD



(2)

RESISTOR DIPS INDICATED WITH * ARE TO BE INSERTED IN BOARD WITH PIN 1 OF DIP IN PIN 9 OF SOCKET. (7 PLACES)

SEE CHART (3)

(1)

-914	JC	4
-913	JF	3
-912	JE	2
-911	JD	1
-XXX	PROM SET JS	# OF DEVICES

MATERIAL	30 DEC 76	PRIME COMPUTER INC FRAMINGHAM, MASS
SEE BOM	J.F. TRAVALINI	STORAGE MODULE CONTROLLER WITH PROMS
		D 4004-XXX M

M	LTR	DATE	REVISION	DR.	CK.
	A	4-11-77	RELEASED	J.F.T.	DJG

SHEET 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41
A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A

SHEET

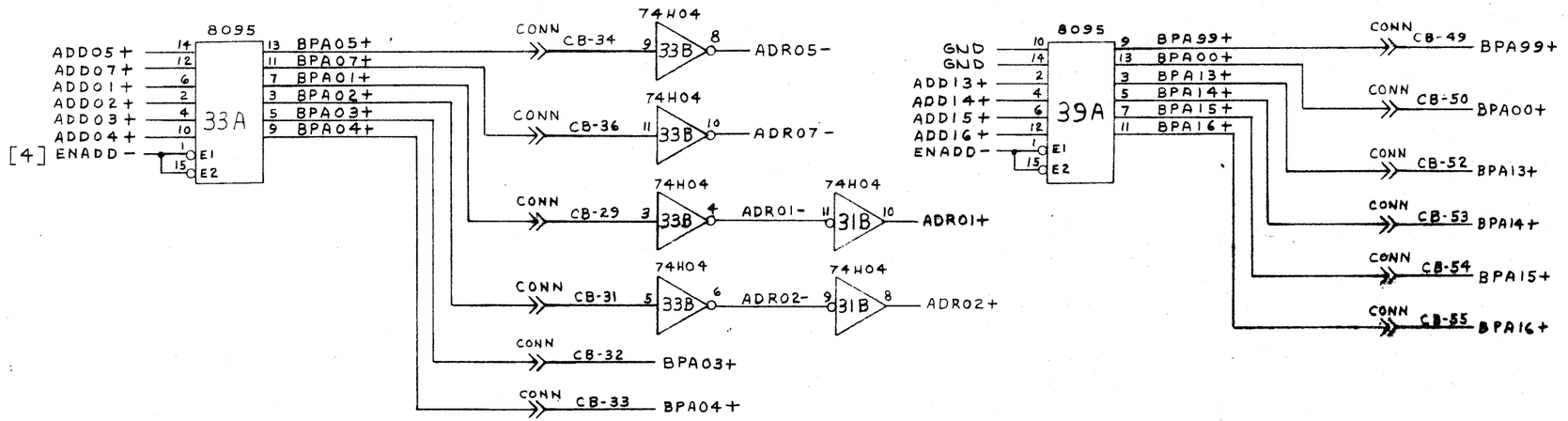
SHEET

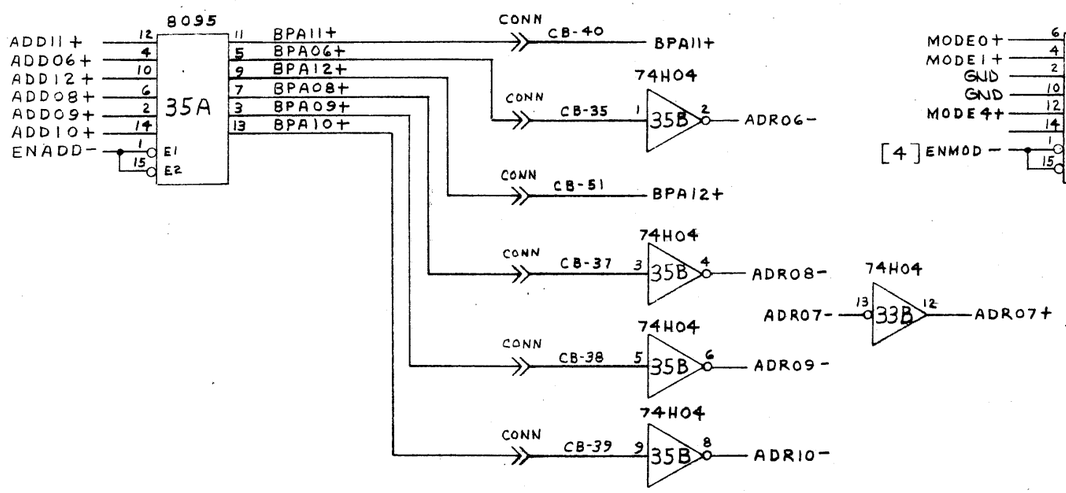
III=01

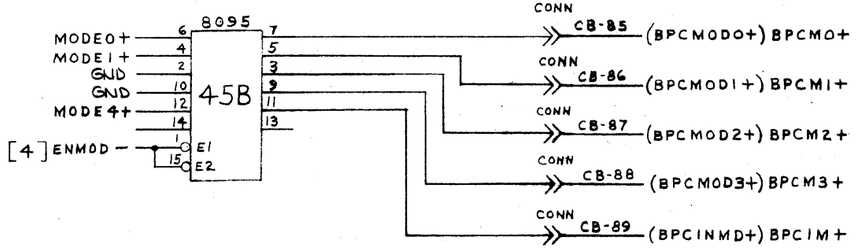
MATERIAL — //	DWN 21 JAN 1977 J. F. TRAVALINI	PRIME COMPUTER, INC. FRAMINGHAM, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK J.G. Travalini 4/11/77 ENG. Derek Gardiner 4-11-77 APPRD	REVISION STATUS SHEET SMC 4004 E.V	
	USED ON NEXT ASSY	SCALE — SHEET 1 OF 41	SIZE C DWG. NO. LBD 2902 REV. A

LBD 2902 A

PRIME COMPUTER, INC.







LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD_ _+		
MODE0+		
MODE1+		
MODE2+		
MODE3+		
MODE4+		

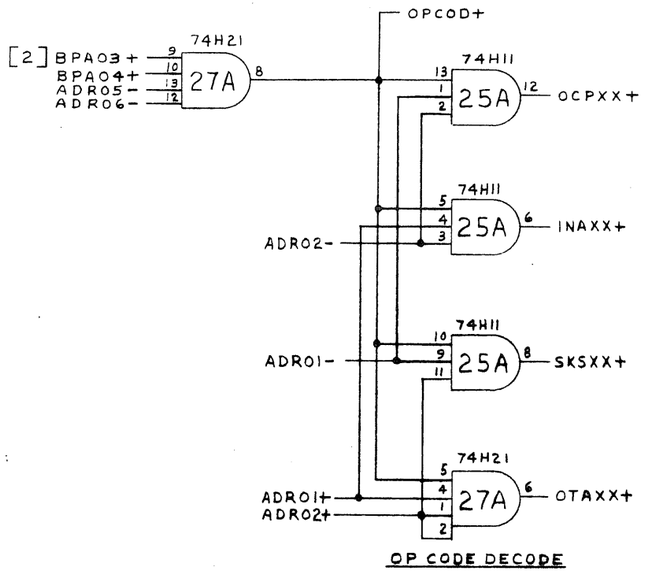
I/O BUS ADDRESS
DRIVERS & RECEIVERS

III-02

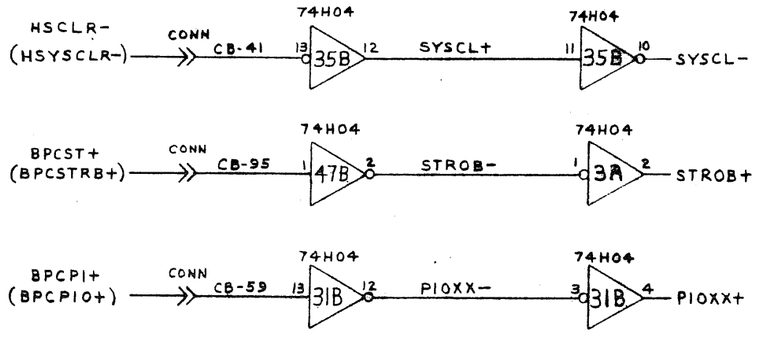
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC ADDRESS AND MODE LINES	
	ENG.		
	APPRD		
USED ON NEXT ASSY	SCALE SHEET 2 OF 41	SIZE C	DWG. NO. LBD2902 REV. A

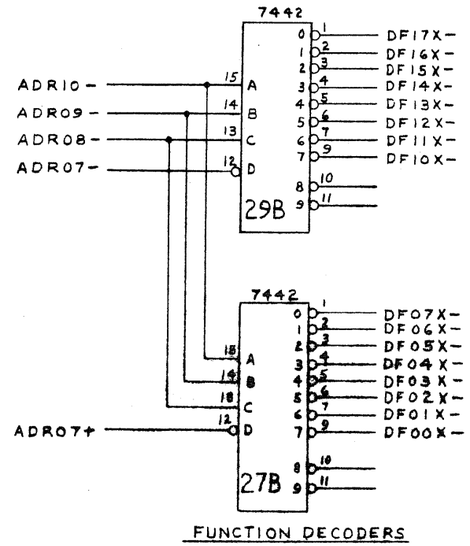
EV

PDF-003

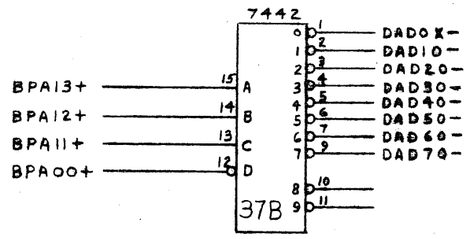


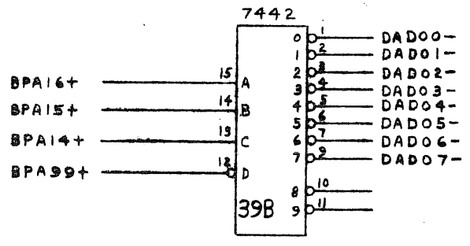
OP CODE DECODE





FUNCTION DECODERS





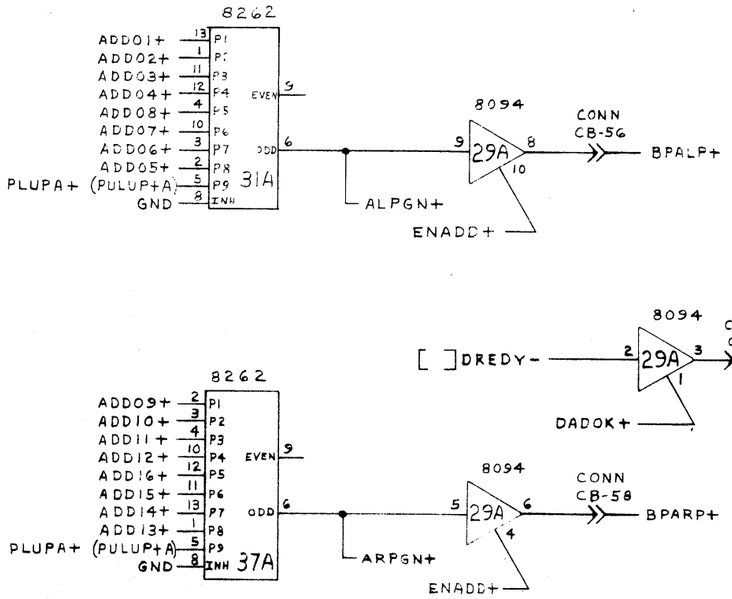
OCTAL ADDRESS DECODERS

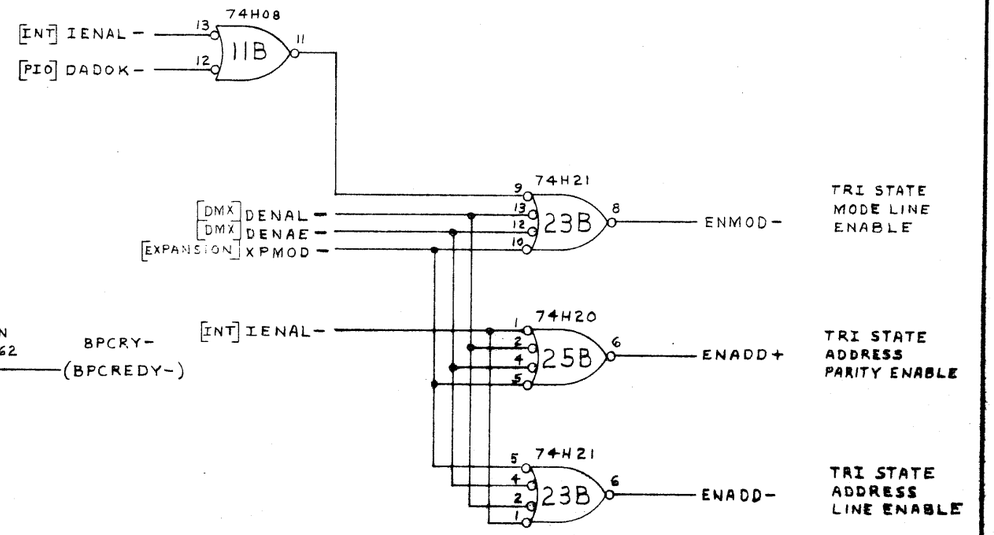
III-03

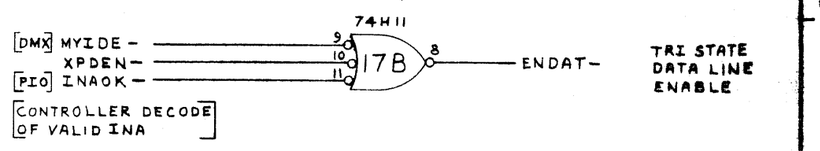
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS DECODING	EV
	APPRD		
	USED ON NEXT ASSY	SCALE SHEET 3 OF 41	SIZE C / DWG. NO. LBD2902 / REV. A

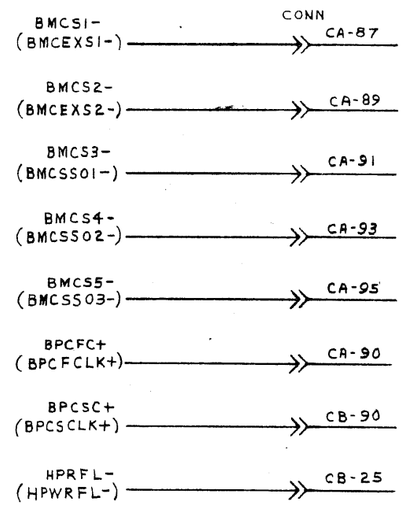
PDF-003

PRIME COMPUTER, INC.

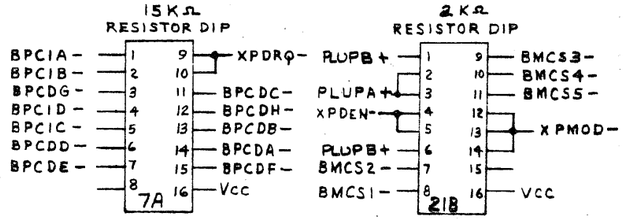








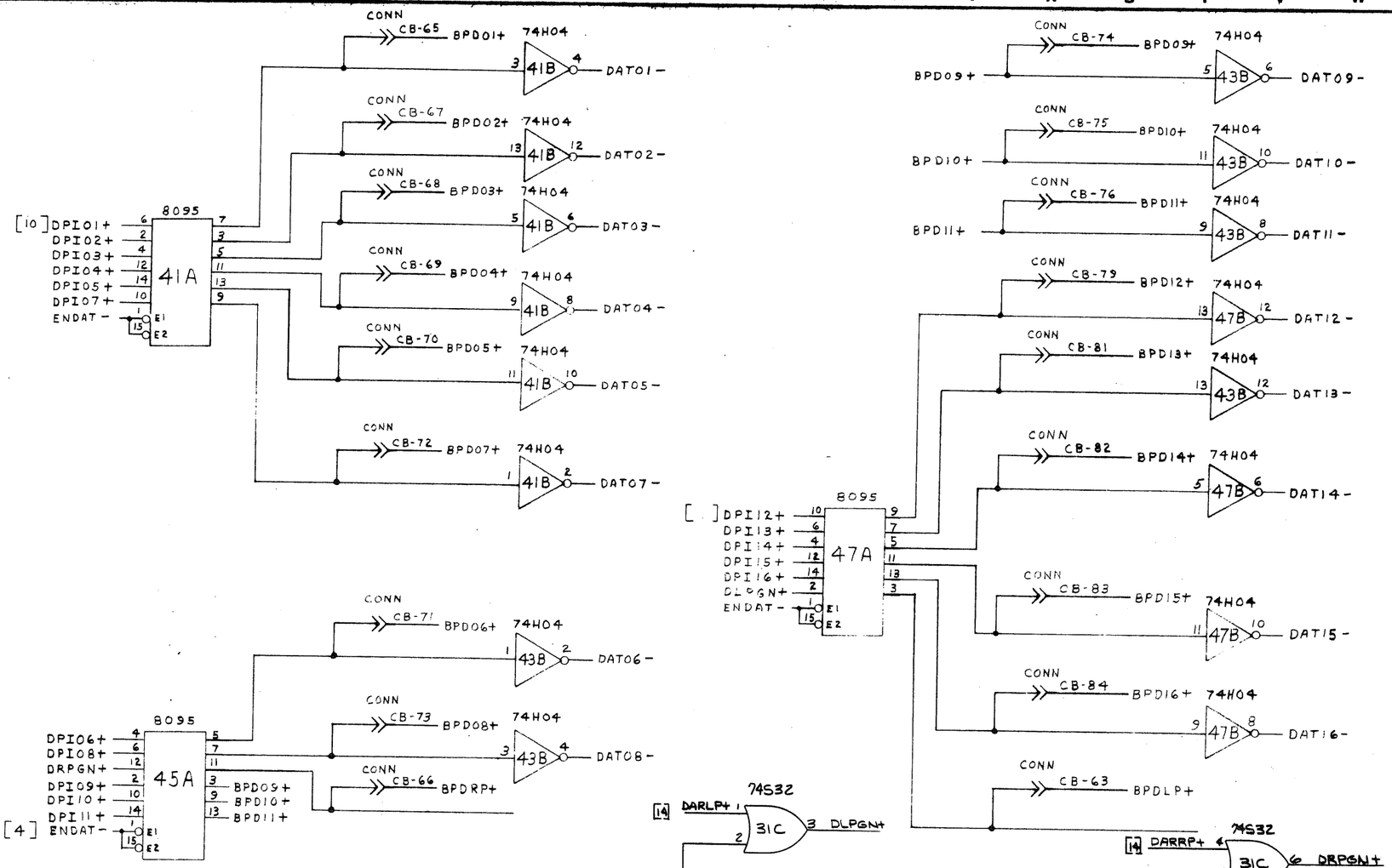
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
COCMD+		
ADD__+		
DADOK-		
XPMOD-		
XPDEN-		
INAOK-		
OTAOK+		
XPDEE-		
DREDY-		
DADOK+		



III-04

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS PARITY EV
	APPRD	
	USED ON	SCALE — SIZE C — DWG. NO. LBD 2902 — REV. A
	NEXT ASSY	SHEET 4 OF 41

PDF-003



LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
DPI +		

III-05

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC DATA BUS LINES EV
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 5 OF 41 · SIZE C · DWG. NO. LBD2902 · REV. A

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74H53
ISHIC-
[ ]HPAIF+
ISPRQ+
IPNRQ+
ISHIC-
IXPIP-
IXPIP+
13B
ICPNP-
CONN CA-17 BPCIO- (BPCIPNO-)

CONN
BPCIA-(BPCIPNA-) CA-18
BPCIB-(BPCIPNB-) CA-19
BPCIC-(BPCIPNC-) CA-20
BPCID-(BPCIPND-) CA-21
74H20 9A
IPNOR-
BPCIPND- ENDS IN THIS CONTROLLER

74H04 11A IPNOR+

IPNOR+
[ ]HPAIF-
74H10 19A GIRQO-
74H00 21A CTIRQ+
74H01 23A
OPEN COLLECTOR
CONN CA-92 BPCIR- (BPCIRQ-)

IENAP-
74H10 19A GCNIR-
74H10 19A
IPNRQ-

BPCOV- (BPCIOVI-) CONN CA-38
74H04 11A ISHIP+
74H00 7B ISHIC-

CONTROLLER NORMAL INTERRUPT REQUEST

74H10 IENAL+ ISPRQ+ 19B KCNSI-
USED TO COUNT OVERRIDE INHIBIT INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED

74H74
PLUPB+
[ ]CNIRQ+
IPNRQ+
IPNRQ-
13A
KIPNR-

74H00 21A XGIRQ-
X1

BPCIN+ (BPCIEN+) CONN CA-16
74H04 11A IENAP-
74H04 11A IENAP+

74H10 ISPRQ- IPNRQ+ IENAL+ 19B CMYIN-
USED TO COUNT NORMAL INTERRUPT CYCLES IN THE CONTROLLER IF NEEDED

BPCPN+ (BPCICPN+) CONN CA-23
74H04 11A ICPNP-
74H08 CINIT- 11B

74H74
PLUPB+
GND
IENAP+
13A
ISPRQ+
ISPRQ-

74H00 ISPRQ- 21A GND
74H01 23A
OPEN COLLECTOR
X2
21A (GND)

CONTROLLER OVERRIDE INHIBIT INTERRUPT REQUEST

74H106 15A
74H00 7B
SIENA-
SIENA+
IENAP+
GND
KIPNR-
PLUPB+
IENAL+
IENAL-

74H00 21A GCNSI-

74H74 15B
PLUPB+ (PULUP+B)
IENAP+
IETCL+
IETCL-

74H11 17B
IPNOR+
ISHIC-
IPNRQ+
LHPAI+

74H106 15A
PLUPB+ (PULUP+B)
IENAP+
GND
HPAIF+
HPAIF-

74H11 17B
CINIT-
KHPAF-

74H74 15B
PLUPB+ (PULUP+B)
IPNOR+
HPAIF+
KHPAI+
KHPAI-

74H55 17A
ISPRQ+
ISHIP+
IPNOR+
IPNRQ+
ISHIC-

74H04 11A KLHII-

BPCHI+ (BPCCHI+) CONN CA-25

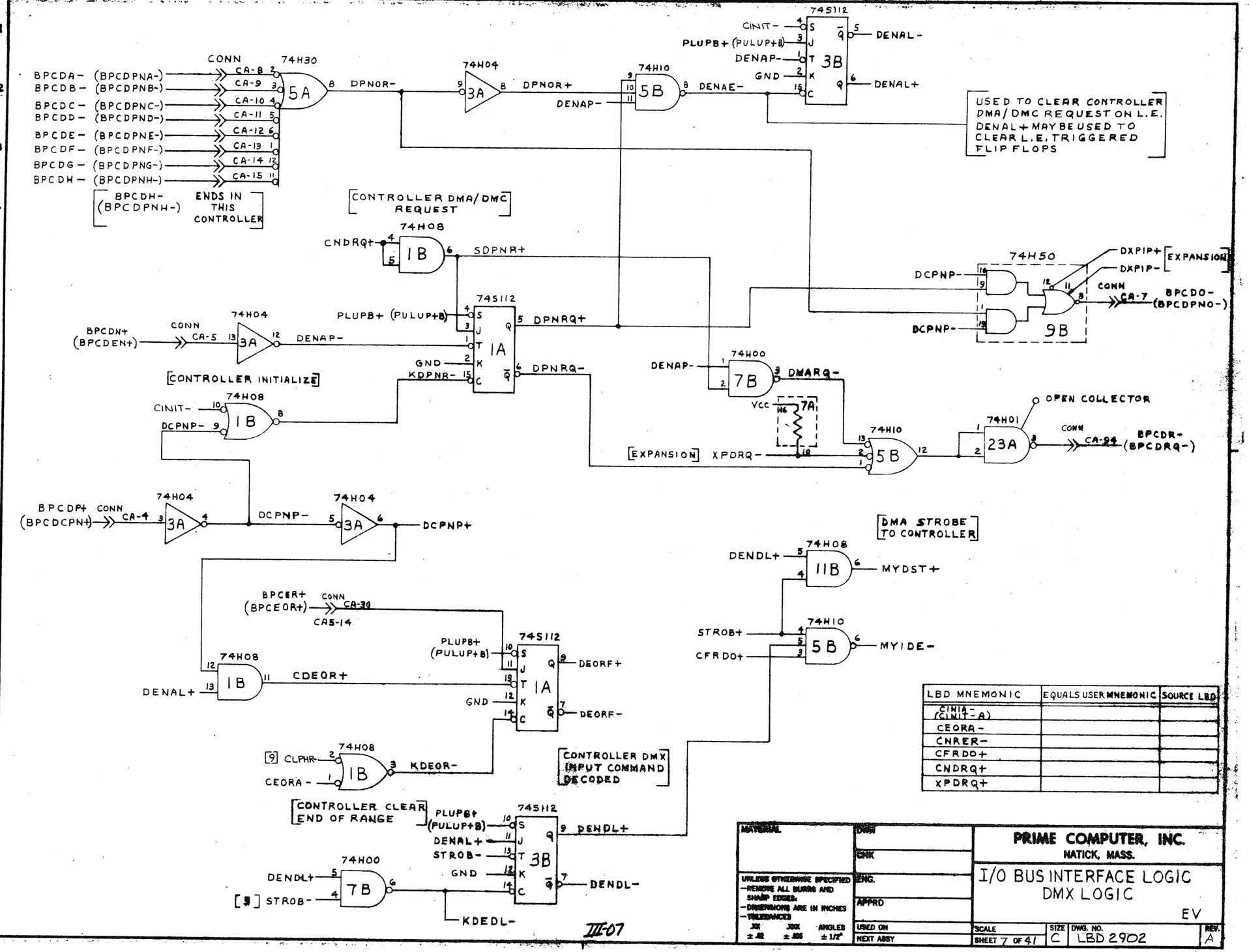
NOTE
1. PRIME INTERRUPT LOGIC WITH OVERRIDE INHIBIT INTERRUPT.
2. CUTX1 TO EXPAND INTERRUPT REQUESTS.
3. CUT X2 TO IMPLEMENT OVERRIDE INHIBIT INTERRUPTS

III-06

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES — DIMENSIONS ARE IN INCHES — TOLERANCES: .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC CONTROLLER INTERRUPT
	ENG.	EV
	APPRD	
	ISSUED ON / NEXT ASSY	SCALE / SHEET 6 OF 41 — SIZE C — DWG. NO. LBD2902 — REV. A

PDF-003

PRIME COMPUTER, INC.

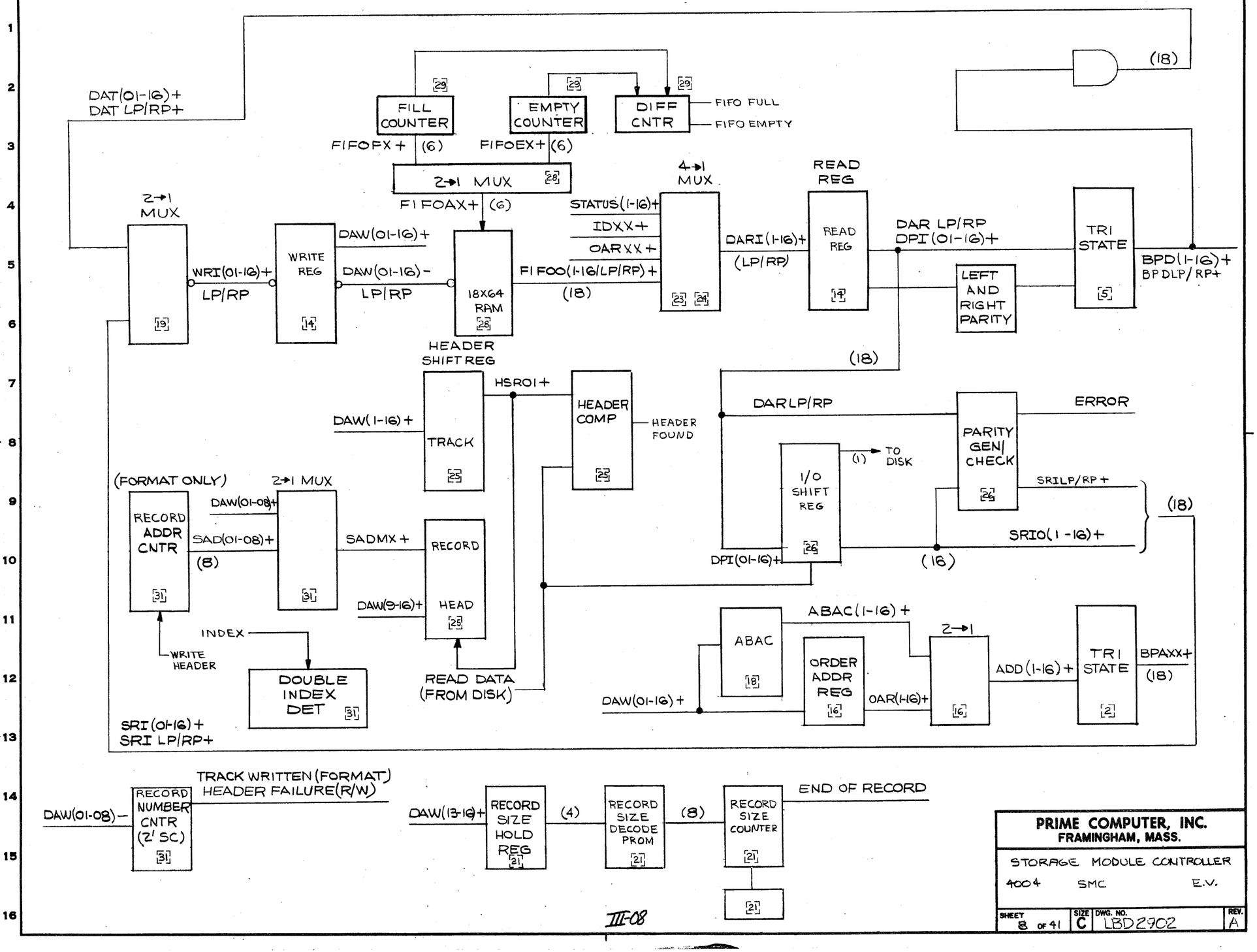


LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIA- (CINIT-A)		
CEORA-		
CNRER-		
CFRDO+		
CNDRQ+		
XPDRQ+		

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES. — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	I/O BUS INTERFACE LOGIC DMX LOGIC EV
	ENG.	
	APPRD	
USED ON / NEXT ASSY	SCALE / SHEET 7 OF 41	SIZE C / DWG. NO. LBD 2902 / REV. A

III-07

PDF-003



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

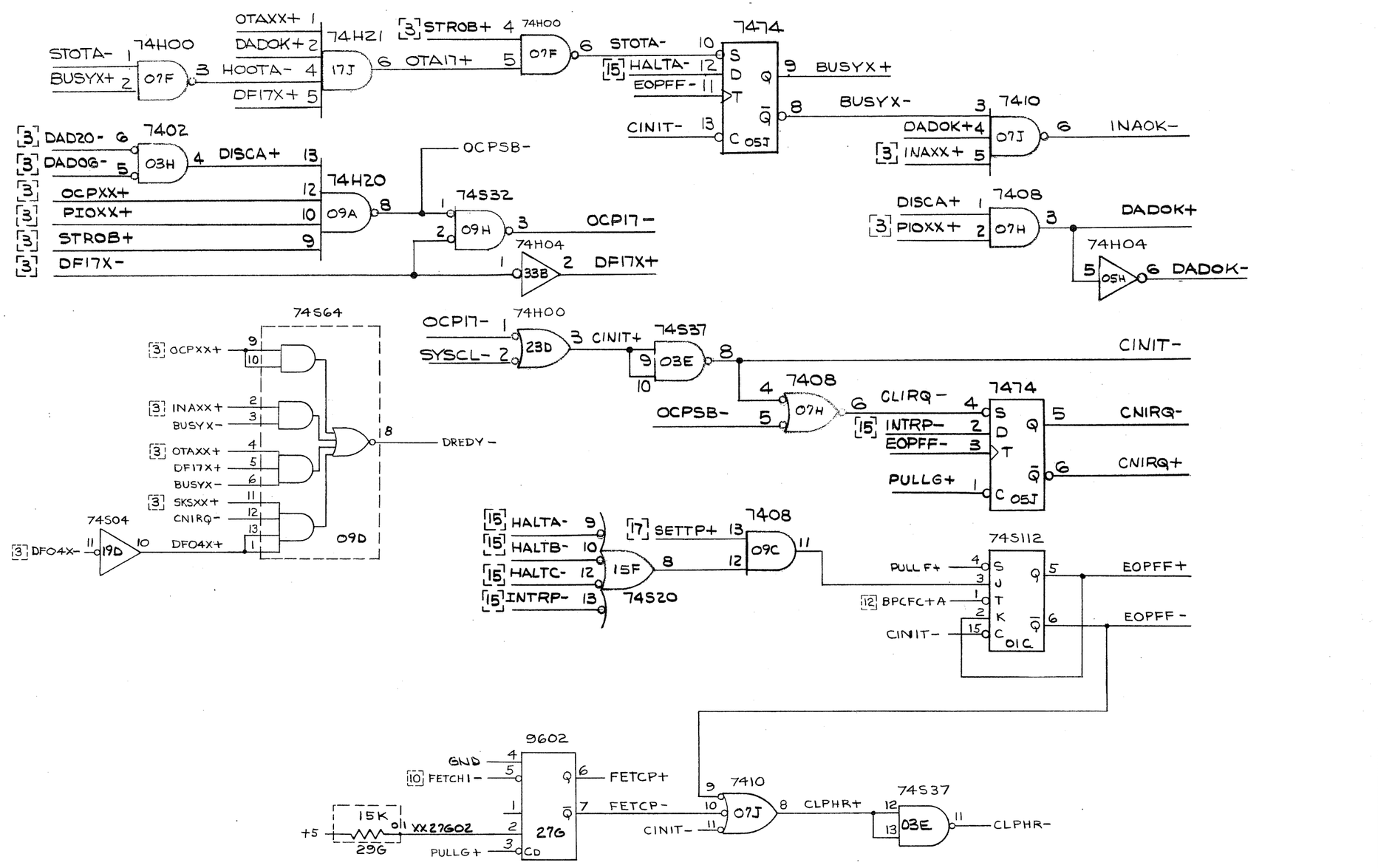
STORAGE MODULE CONTROLLER

4004 SMC E.V.

SHEET	SIZE	DWG. NO.	REV.
8 OF 41	C	LBD2702	A

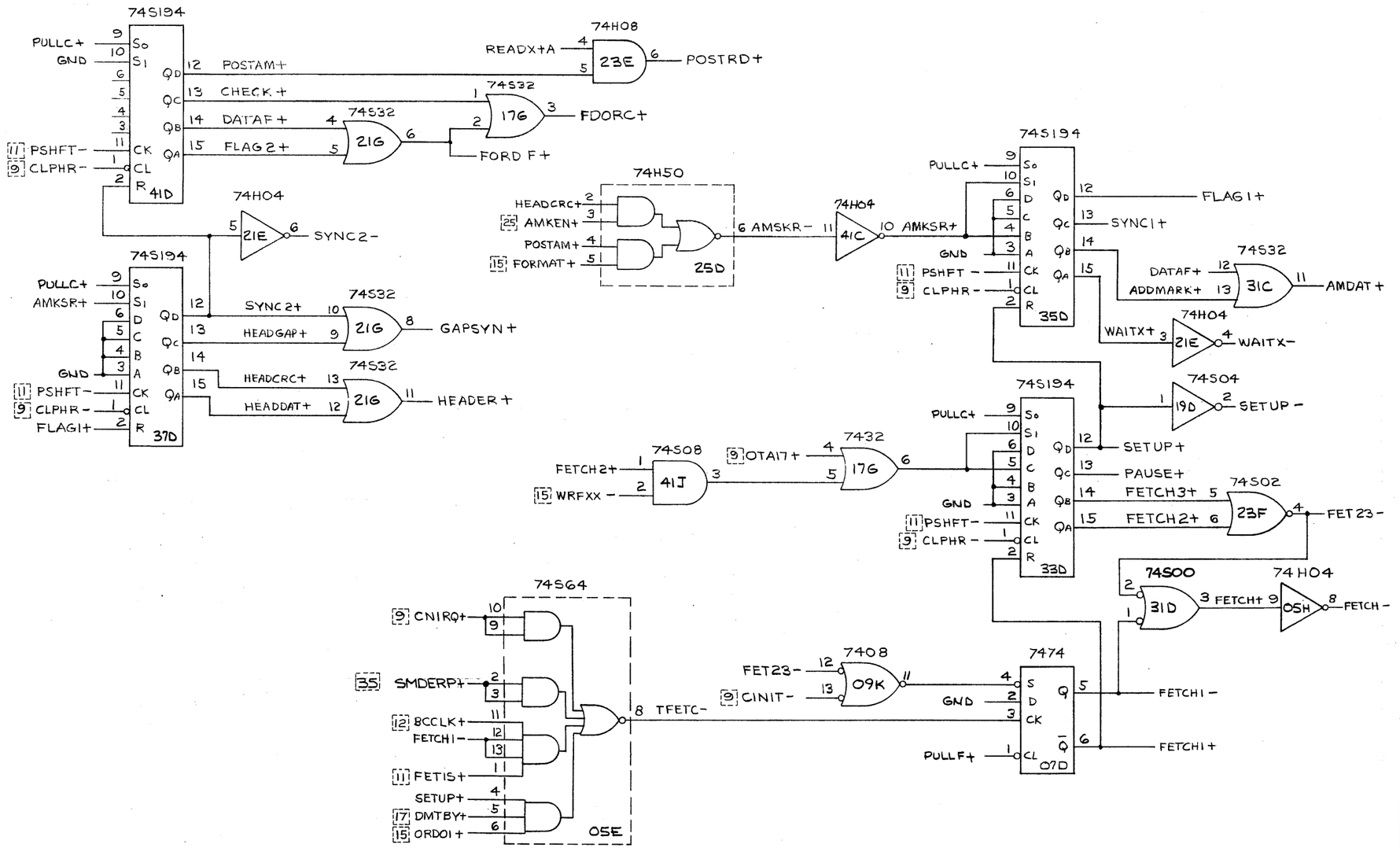
III-08

PDF-003



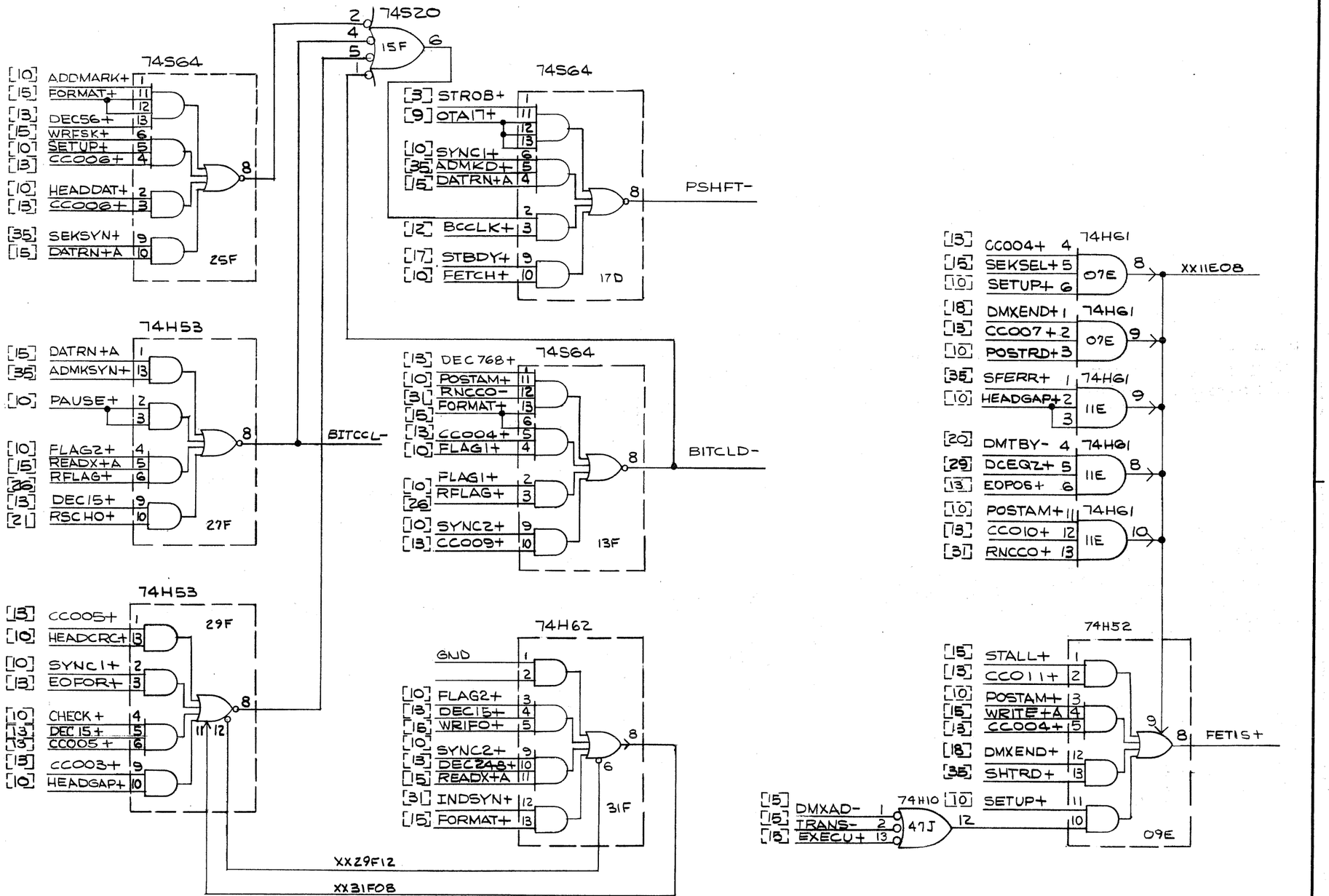
PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
PIO AND INTERRUPT LOGIC	
SMC 4004	E.V.
SHEET 9 OF 41	SIZE C | DWG. NO. LBD2702 | REV. A

PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
PHASE REGISTER			
SMC 4004		E.V.	
SHEET 10 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

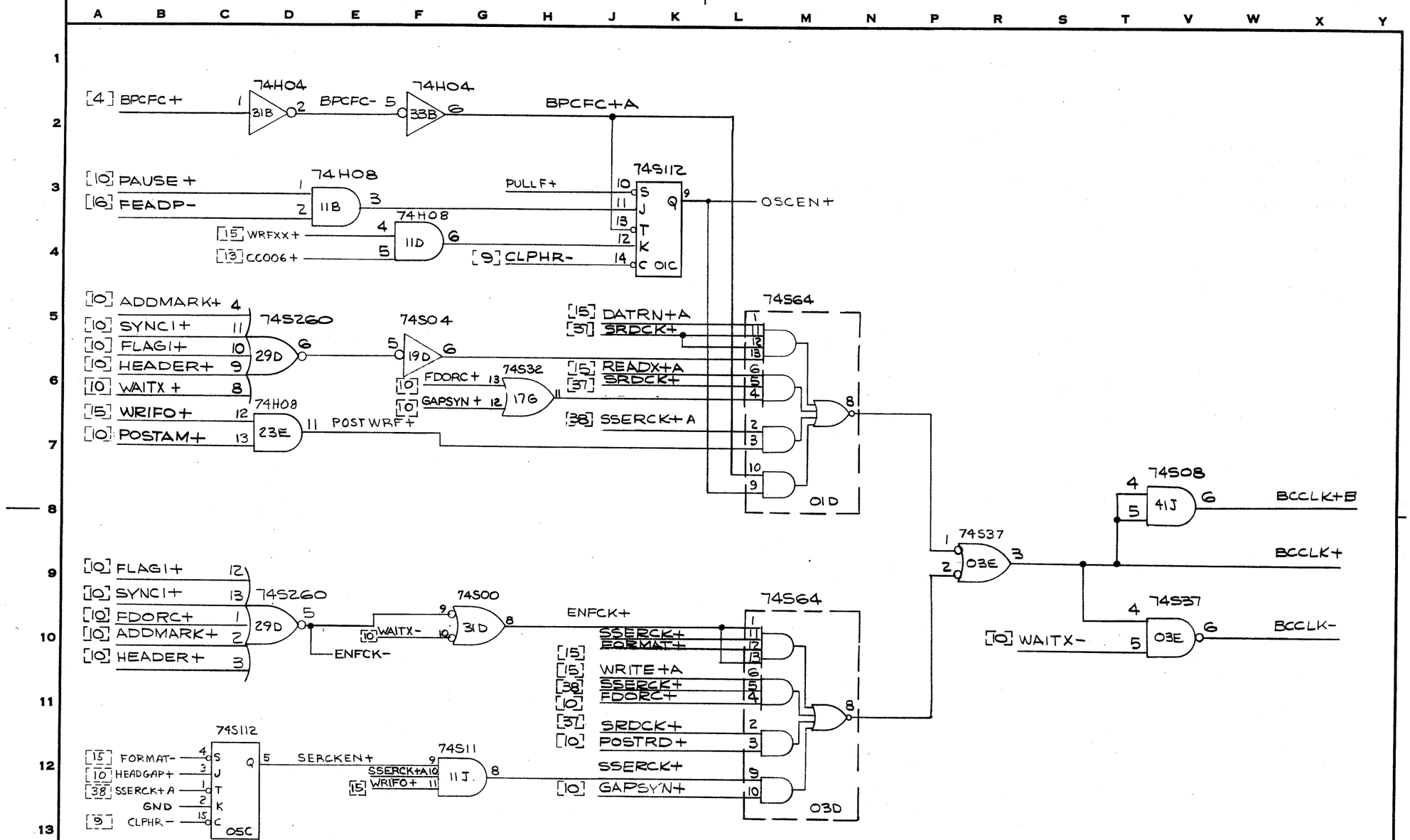
PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
PHASE REGISTER GATING			
SMC 4004		E.V.	
SHEET 11 OF 41	SIZE C	DWG. NO. LBD 2702	REV. A

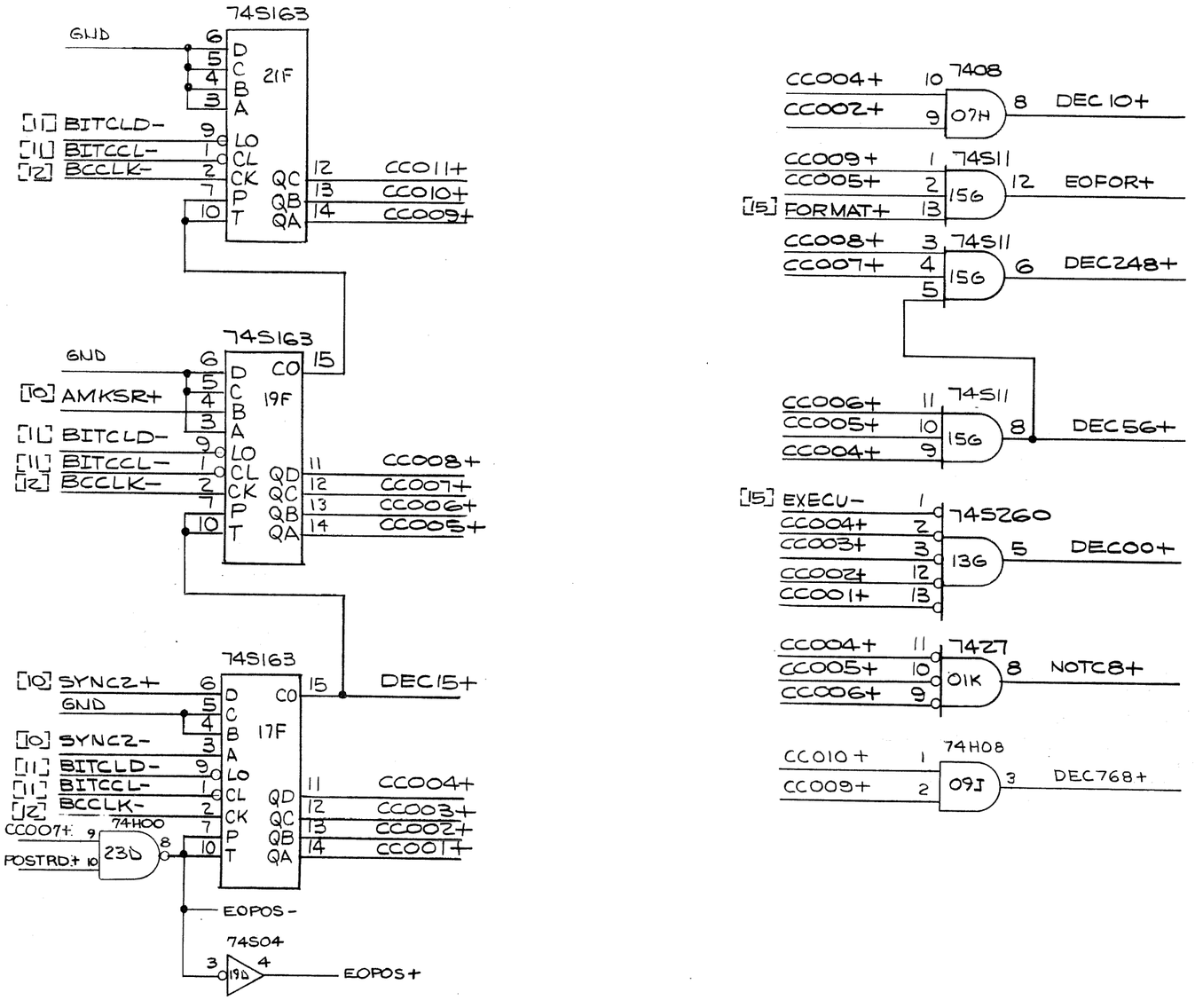
PDF-003

PRIME COMPUTER, INC.



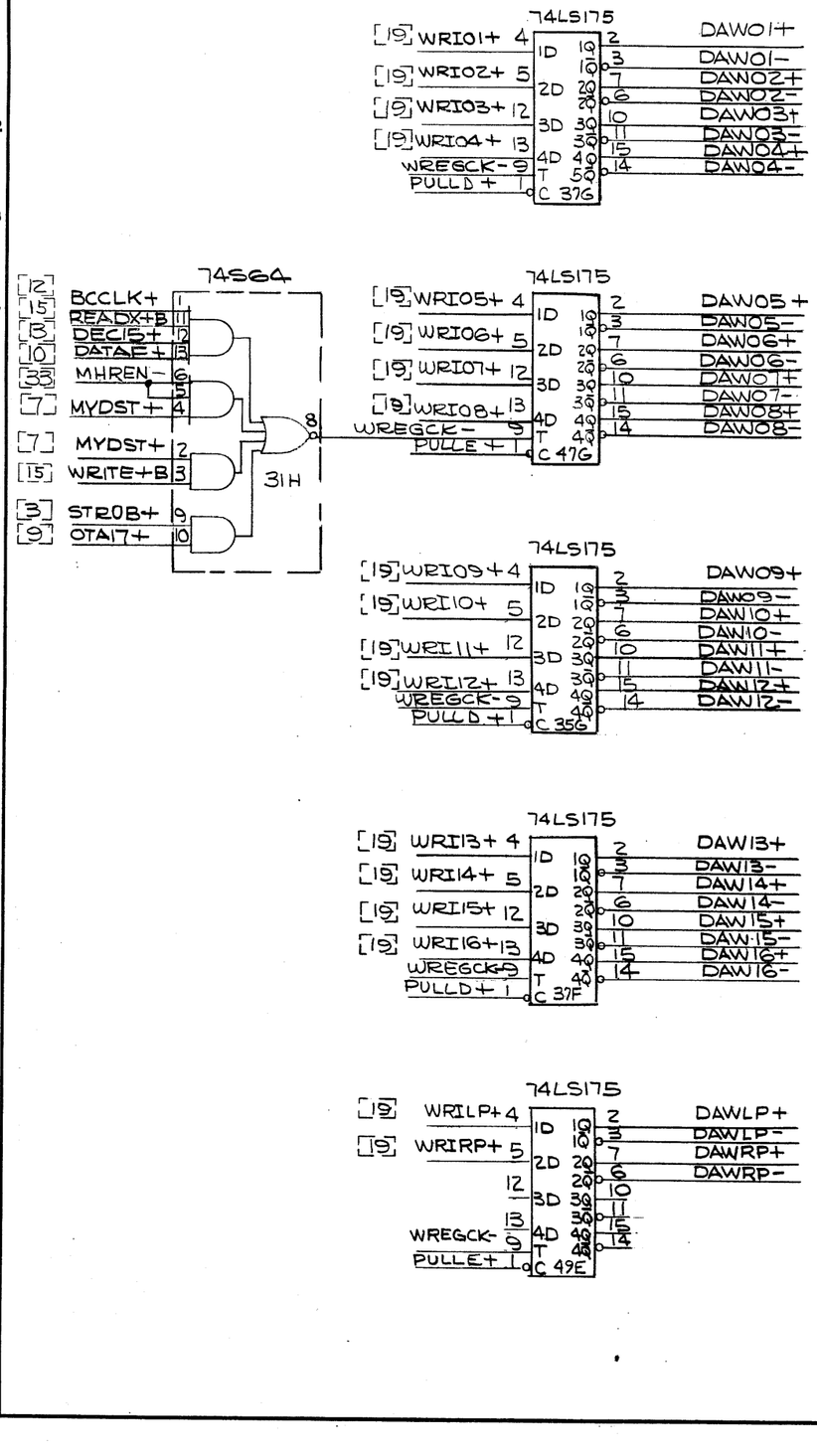
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
CLOCK LOGIC			
SMC 4004 E.V.			
SHEET 12 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

PDF-003



PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
BIT COUNTER	
SMC 4004	E.V.
SHEET 13 OF 41	SIZE C · DWG NO LBD 2702 · REV A

PDF-003



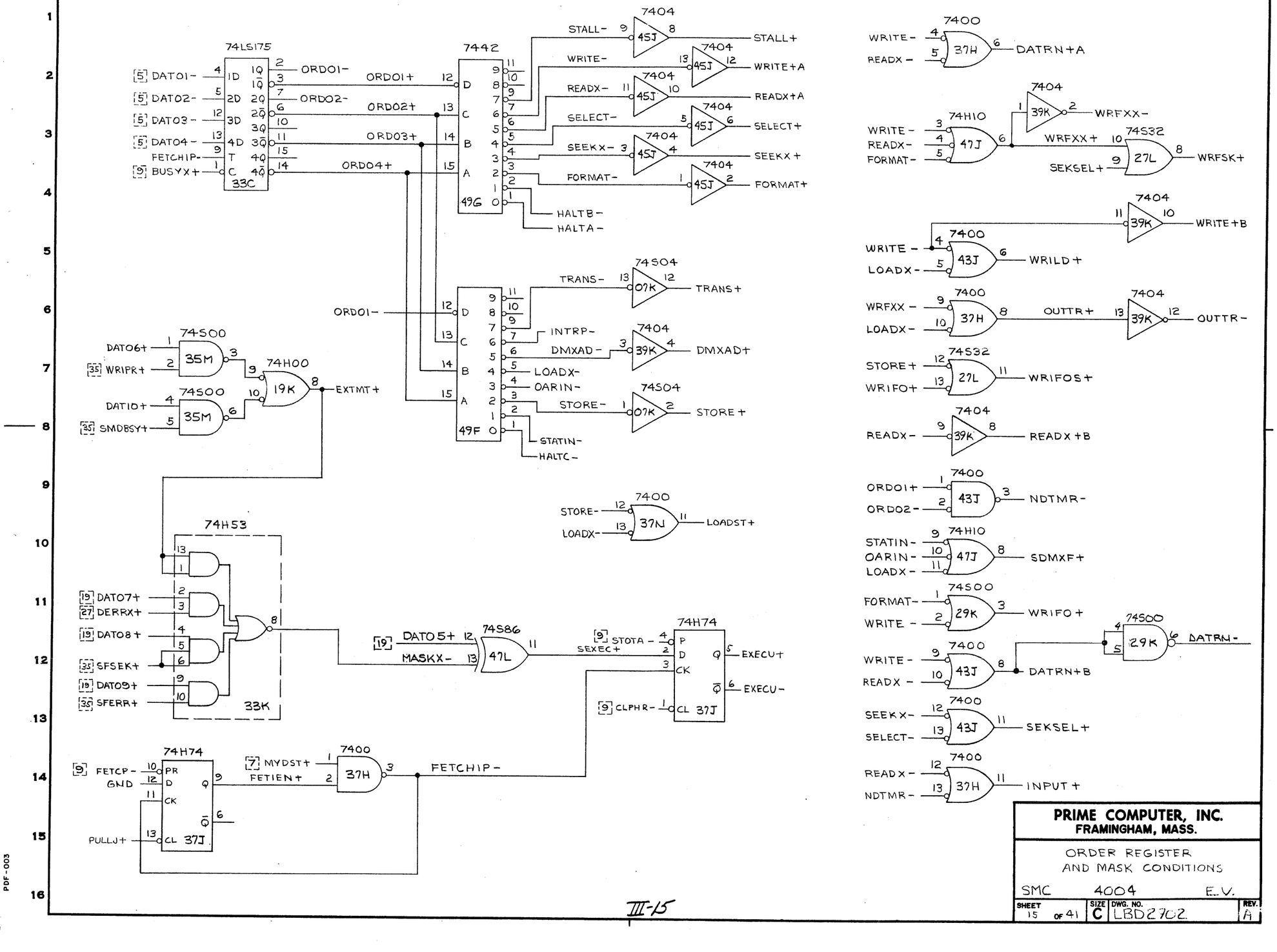
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

WRITE & READ REGISTERS

SMC 4004 E.V.

SHEET	SIZE	DWG. NO.	REV.
14 OF 41	C	LBD2902	A

PDF-003



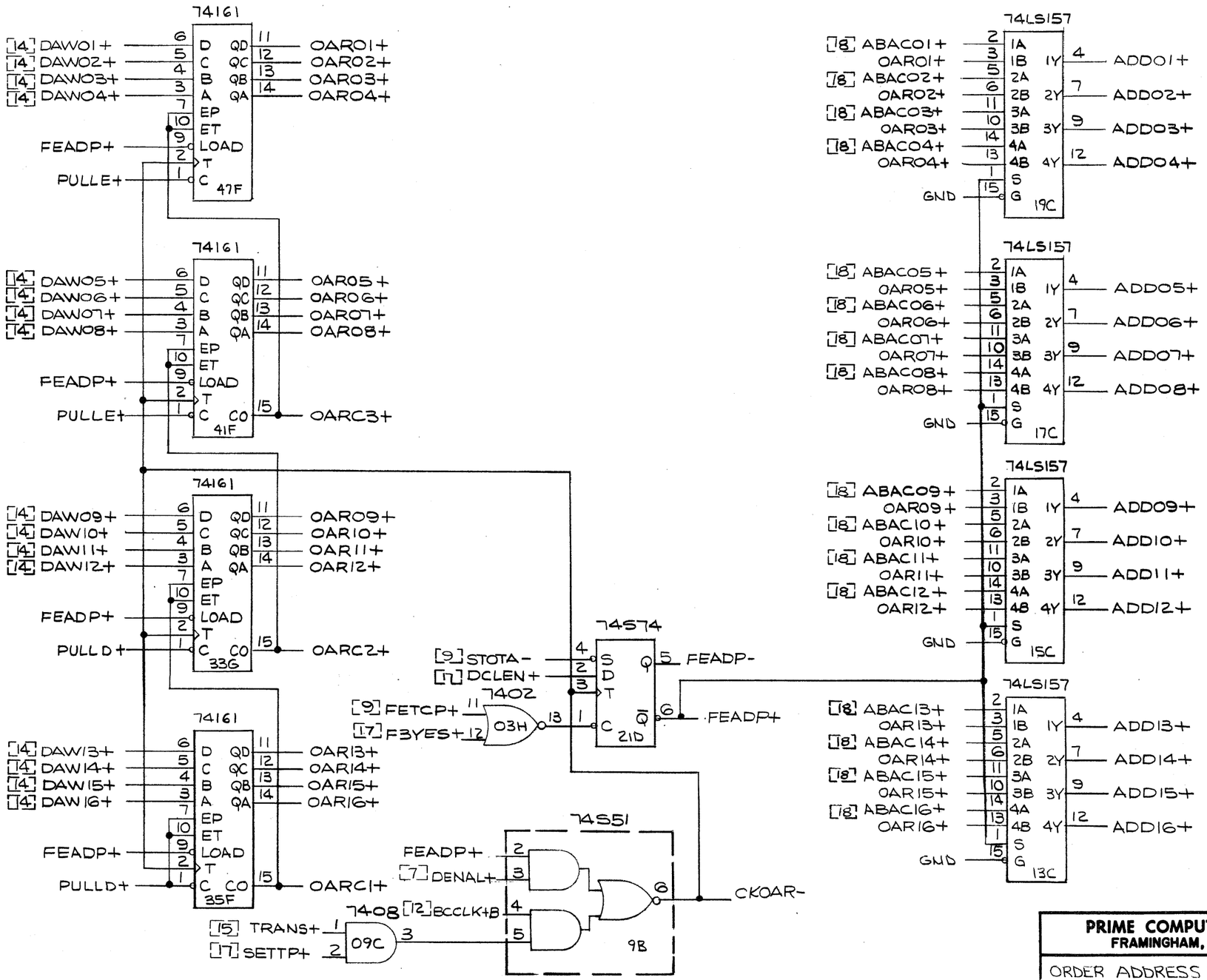
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ORDER REGISTER
AND MASK CONDITIONS

SMC 4004 E.V.

SHEET 15 OF 41 | SIZE C | DWG. NO. LBD2702. | REV. A

PDF-003



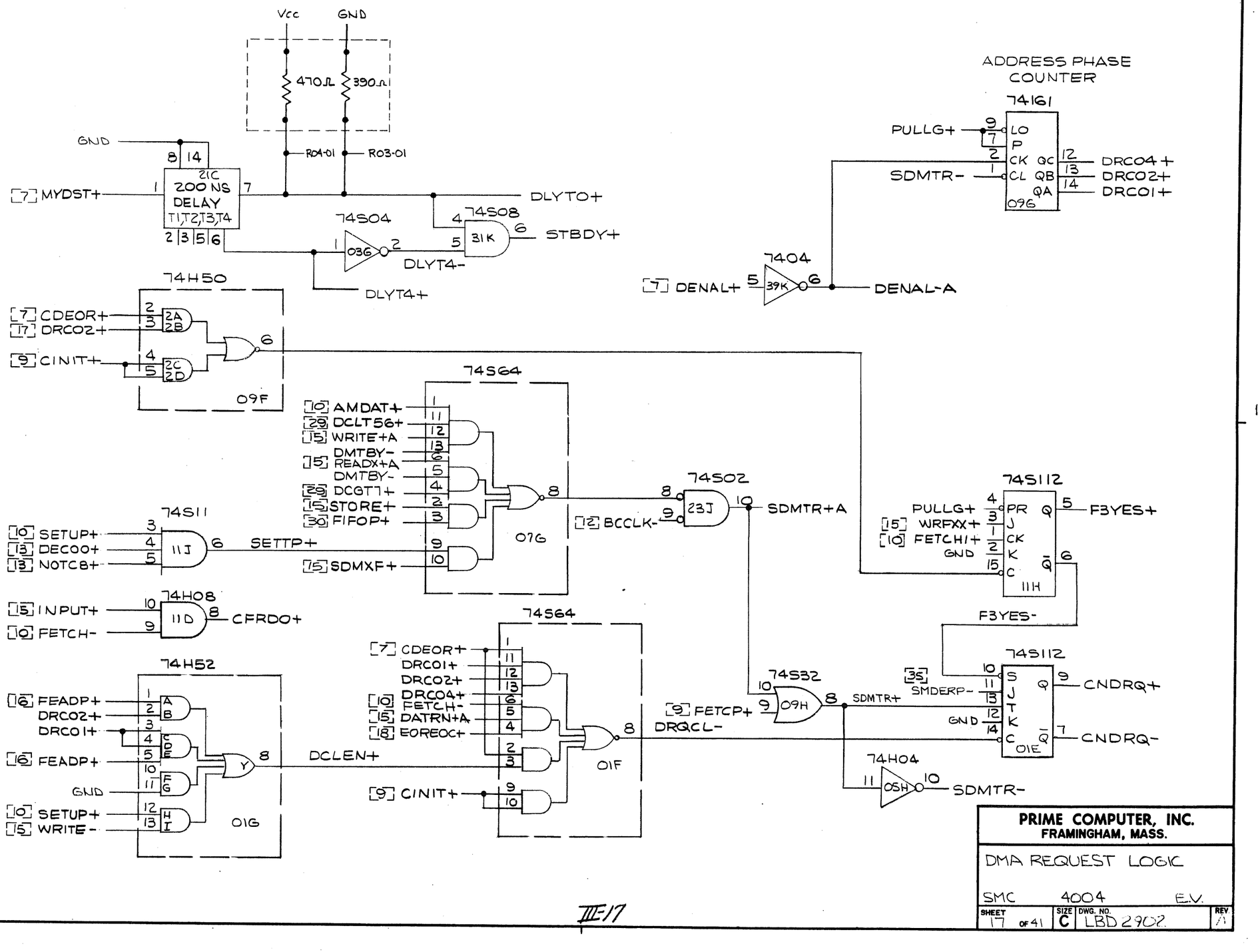
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ORDER ADDRESS REG & ADDRESS INPUT MPX

SMC 4004 E.V

SHEET	SIZE	DWG. NO.	REV.
16 OF 41	C	LBD2902	A

PDF-003



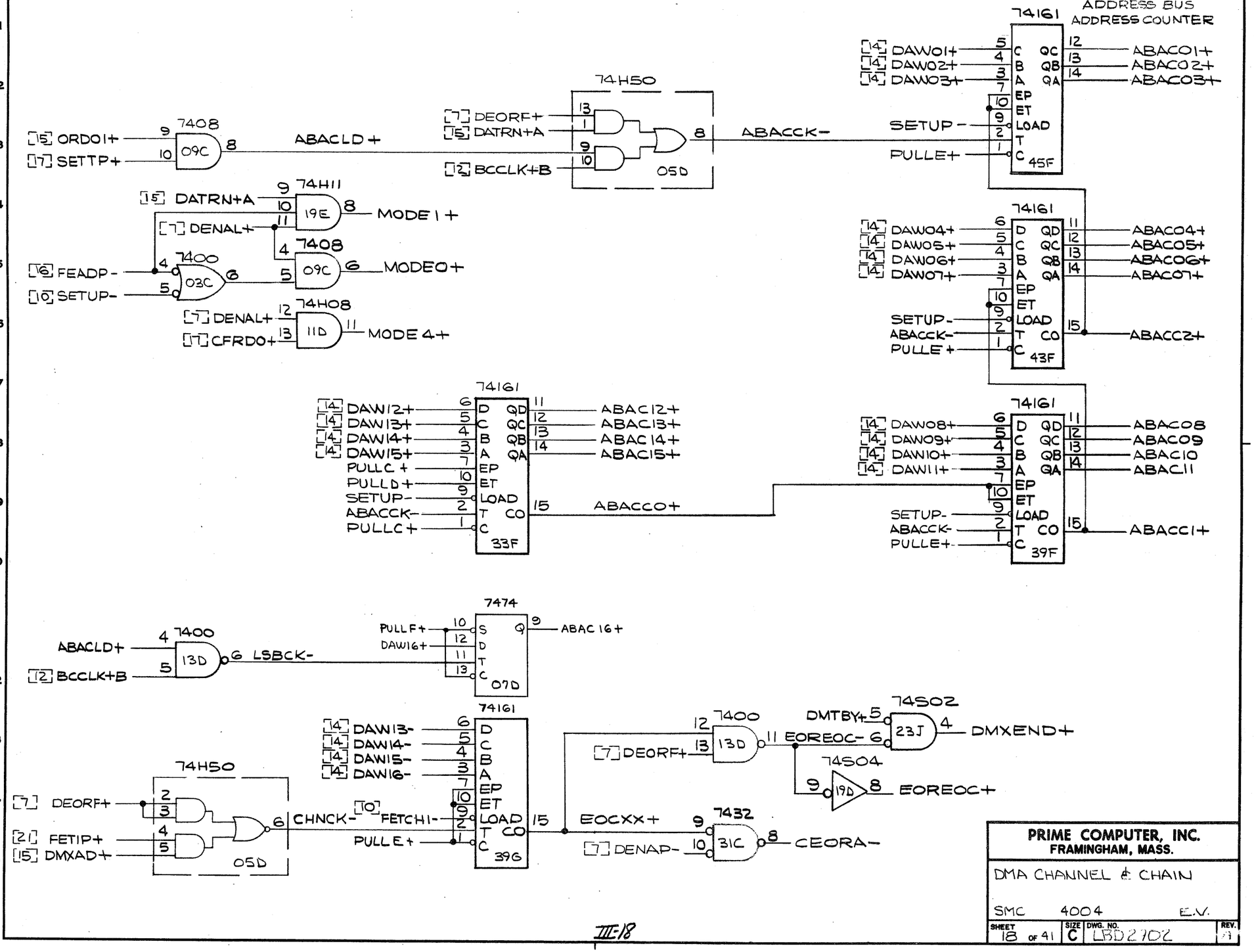
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

DMA REQUEST LOGIC

SMC 4004 E.V.

SHEET	SIZE	DWG. NO.	REV.
17 OF 41	C	LBD 2902	A

PDF-003



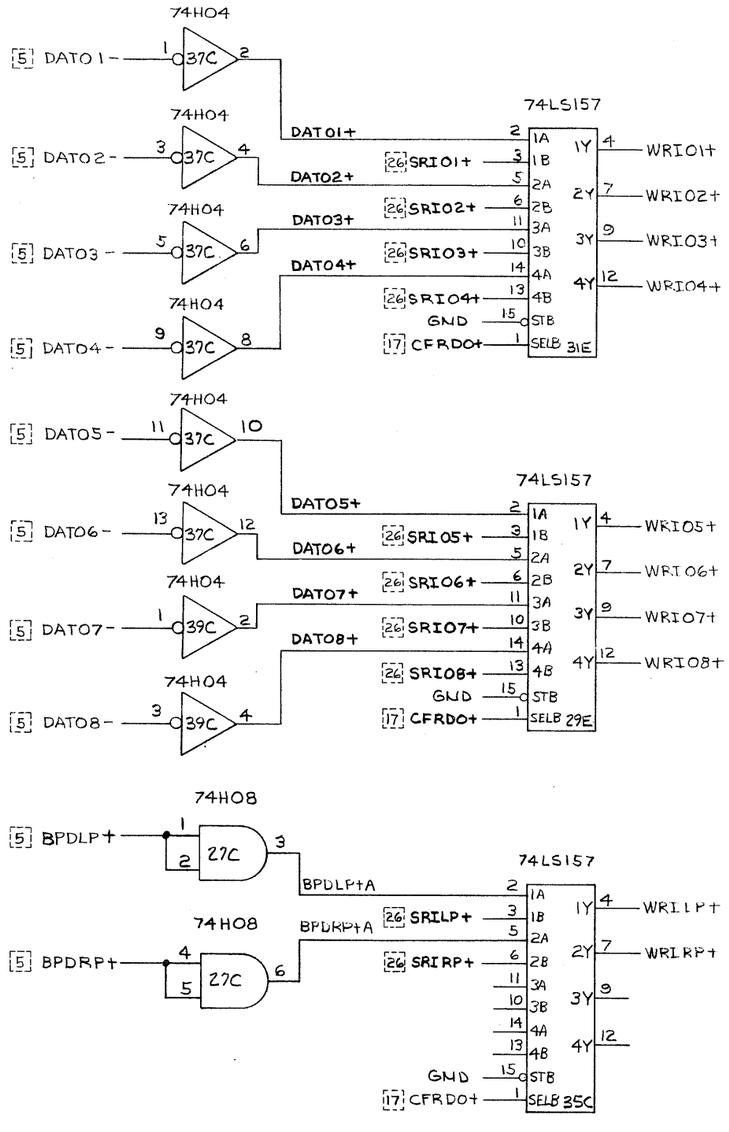
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

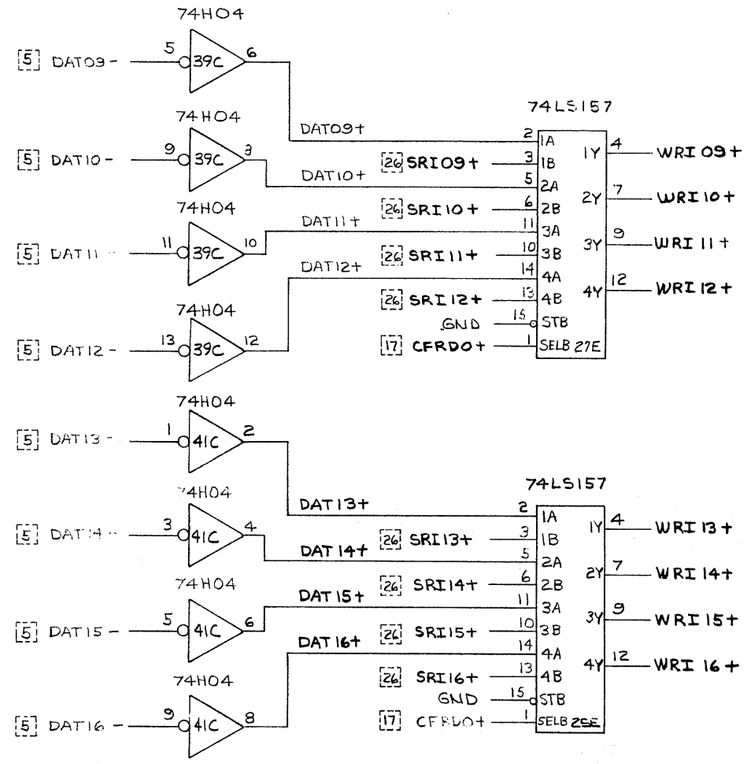
DMA CHANNEL & CHAIN

SMC 4004 E.V.

SHEET 18 OF 41 | SIZE C | DWG. NO. LBD2702 | REV. A

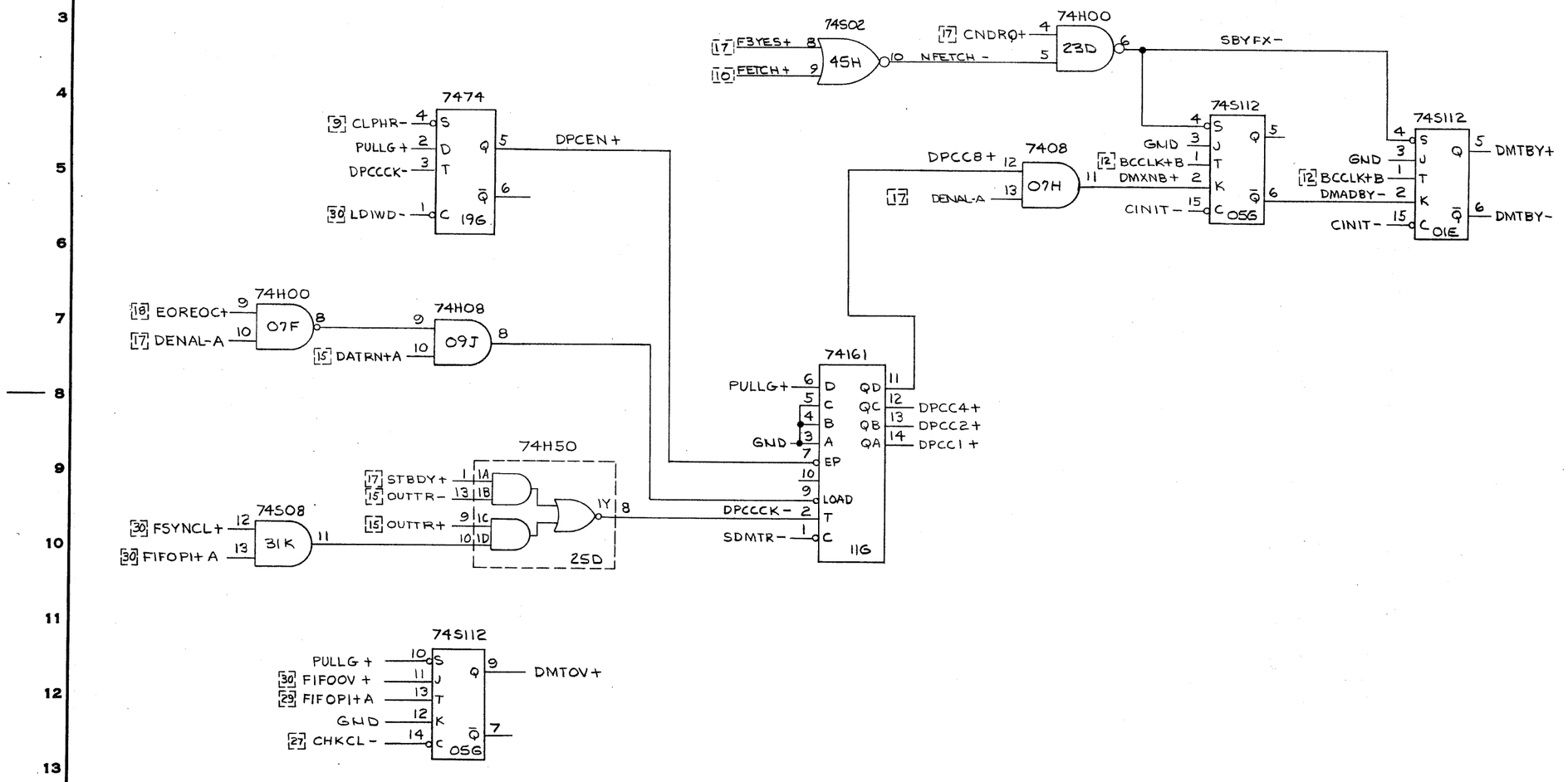
PDF-003





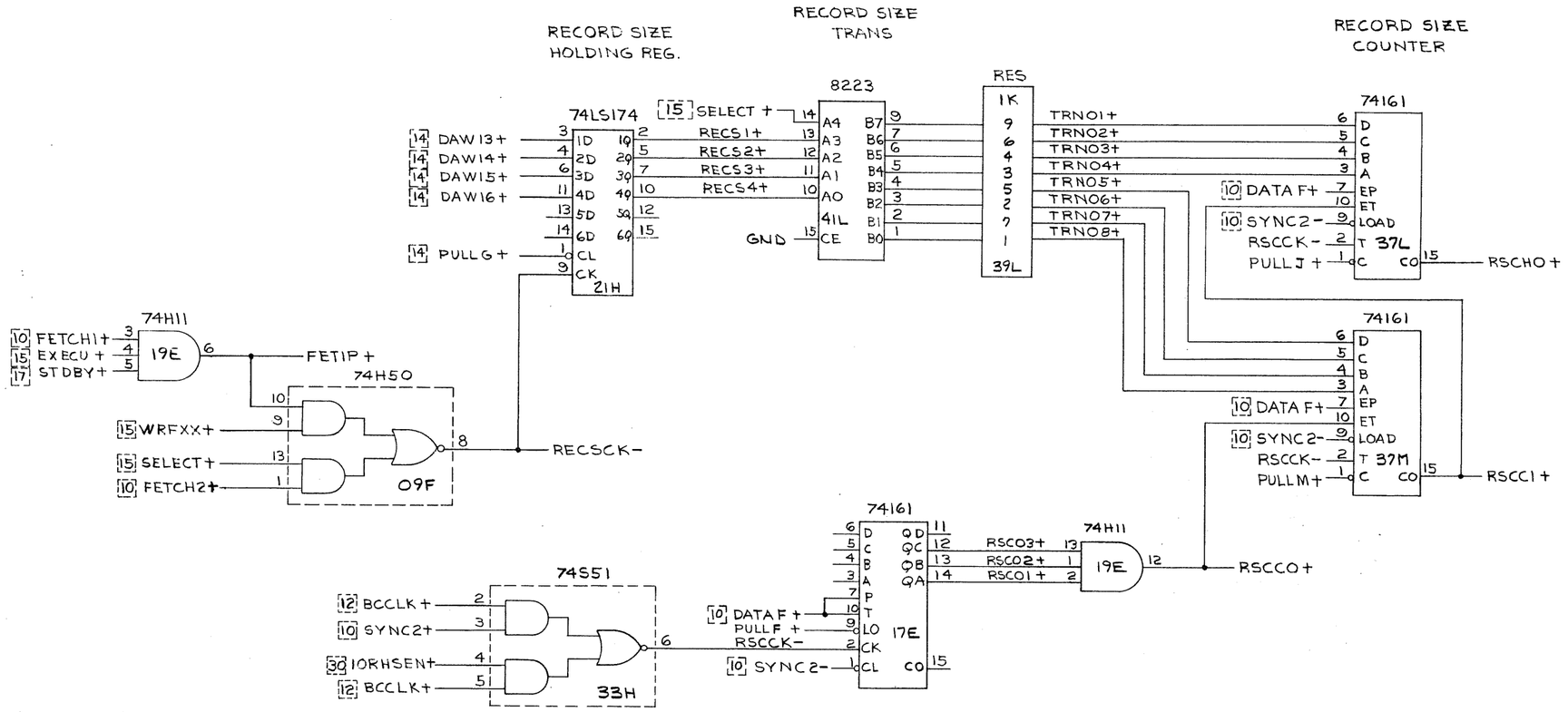
PDF-003

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
WRITE REGISTER INPUT MUX			
SMC 4004 E.V.			
SHEET 19 OF 41	SIZE C	DWG. NO. LBD2702	REV. A



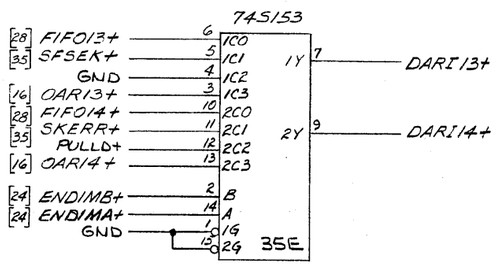
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DMA BUSY AND OVERUN			
SMC 4004		E.V.	
SHEET 20 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

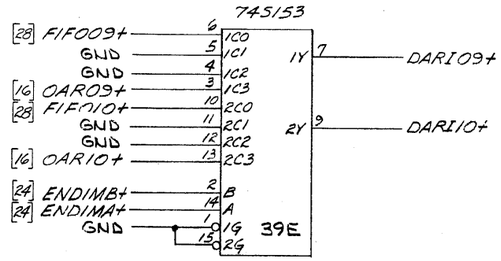
PDF-003

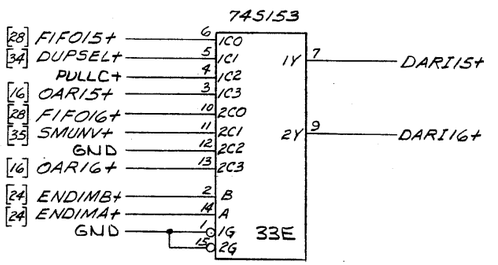


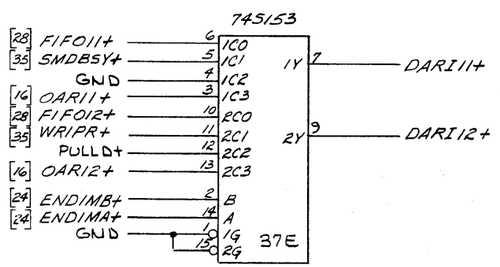
PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
RECORD SIZE COUNT			
SMC 4004 E.V.			
SHEET 21 OF 41	SIZE C	DWG. NO. LBD2702	REV. A

PDF-003







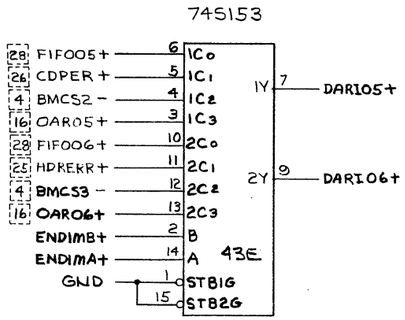


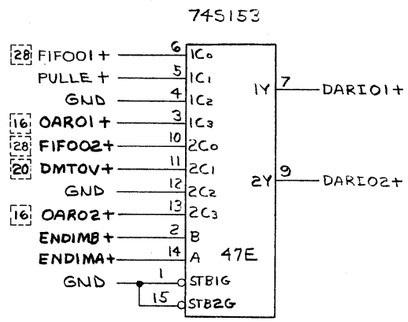
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

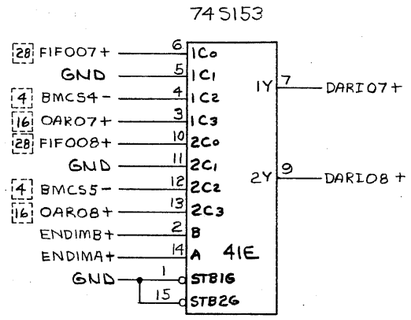
DATA TO READ REG
(RIGHT BYTE)
SMC 4004 E.V.

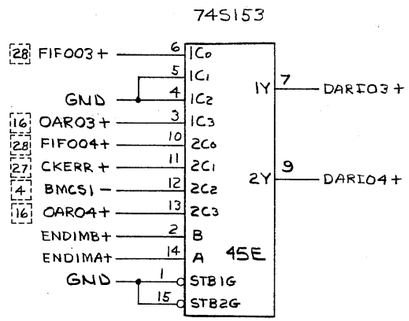
SHEET	SIZE	DWG. NO.	REV.
23 OF 41	C	LBD 2702	A

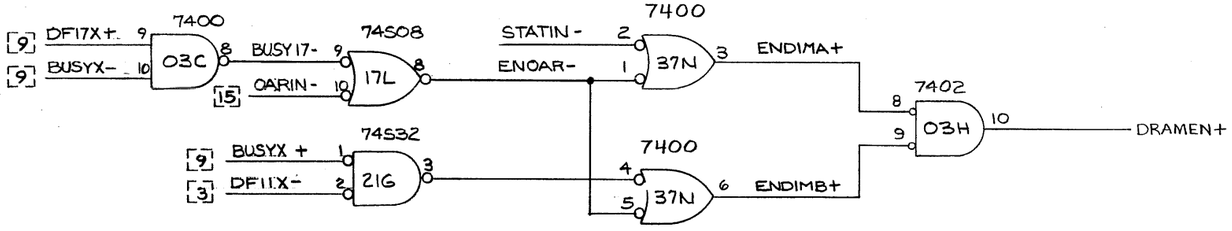
PDF-003





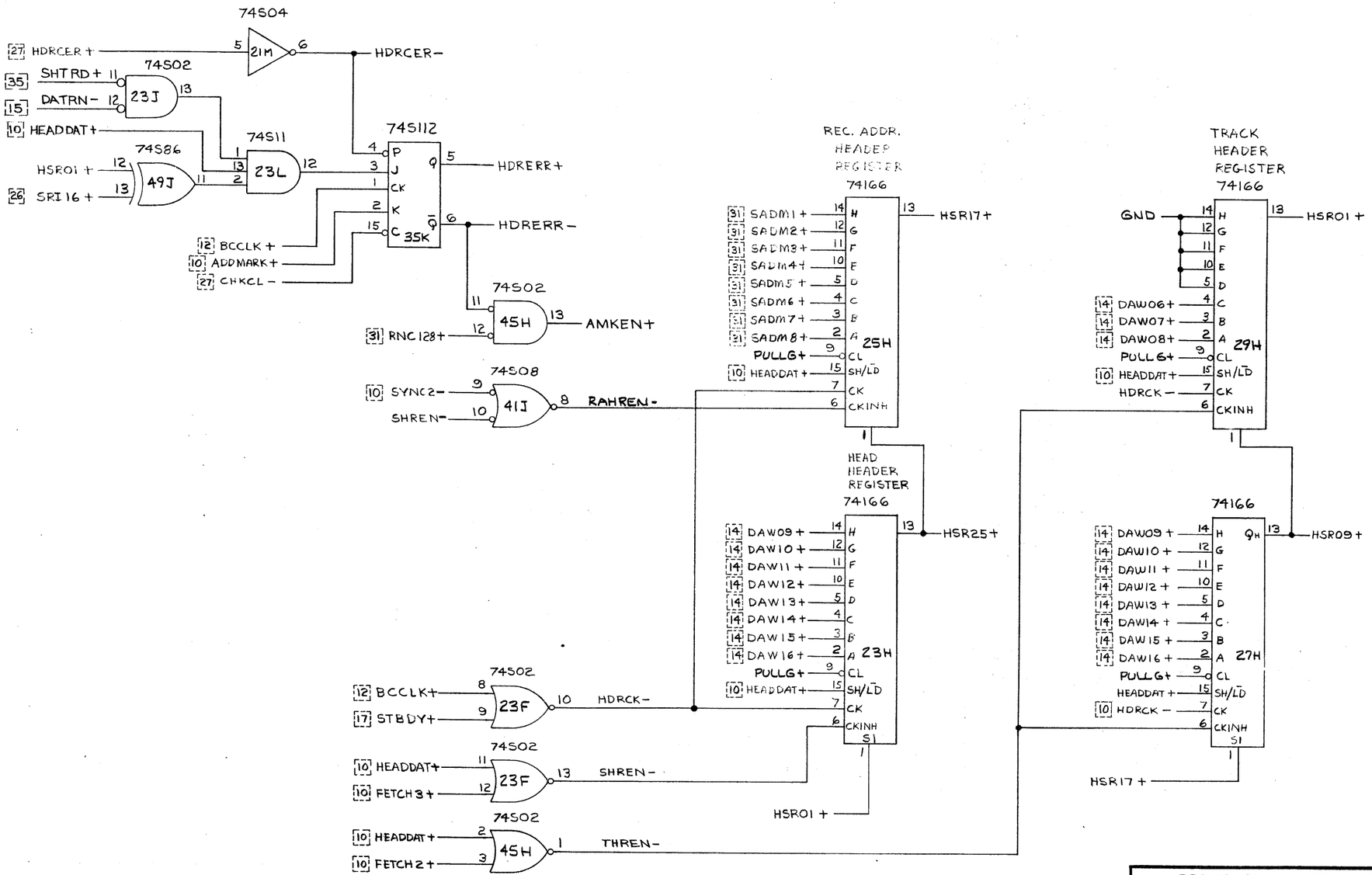






PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DATA TO READ REG (LEFT BYTE)			
SMC 4004 E.V.			
SHEET 24 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

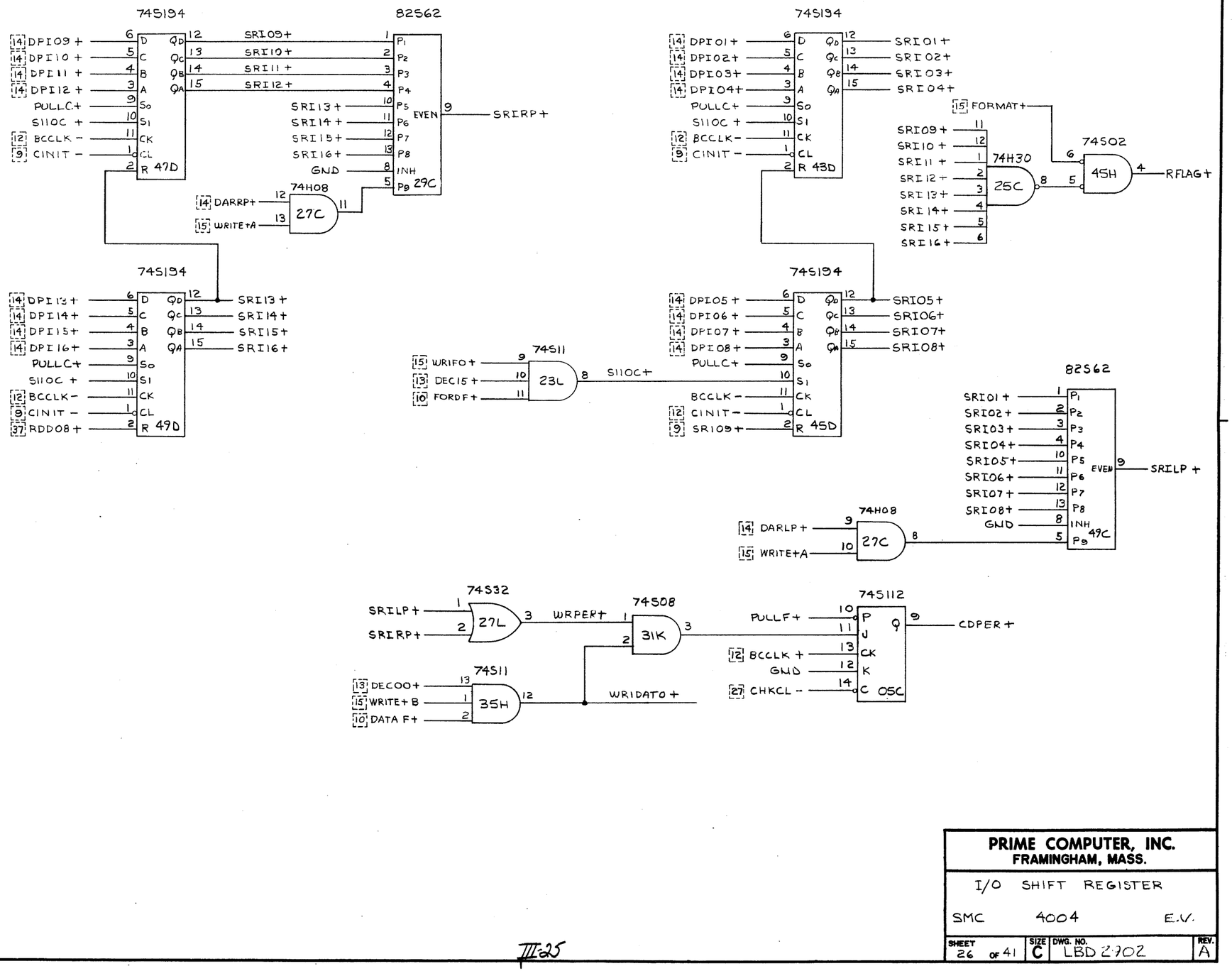
PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
HEADER REGISTER			
SMC 4004 E.V.			
SHEET 25 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

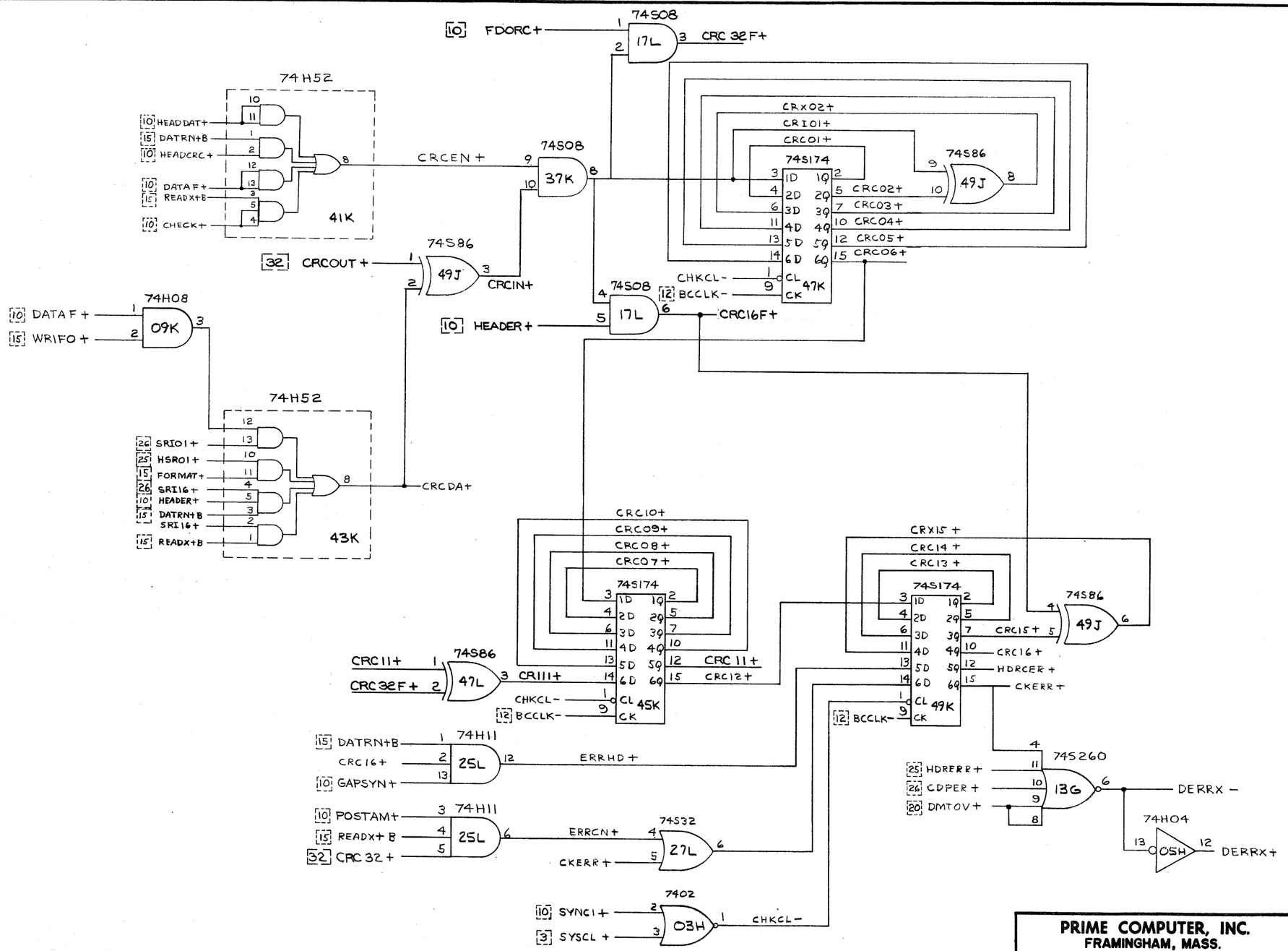
III-24

PDF-003



PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
I/O SHIFT REGISTER	
SMC 4004	E.V.
SHEET 26 OF 41	SIZE C · DWG. NO. LBD 2702 · REV. A

PDF-003



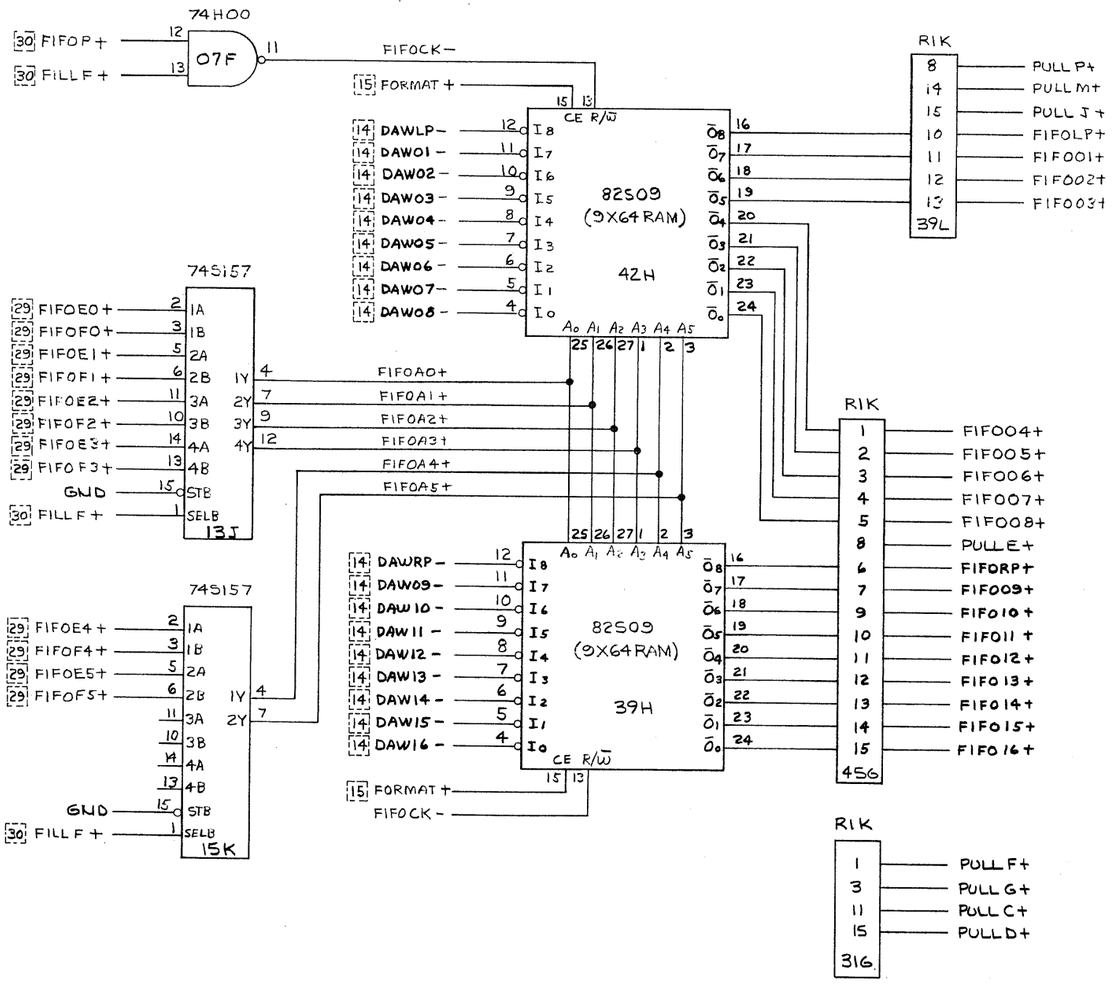
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CHECK REGISTER LEFT

SMC 4004 E.V.

SHEET	SIZE	DWG. NO.	REV.
27 OF 41	C	LBD2902	A

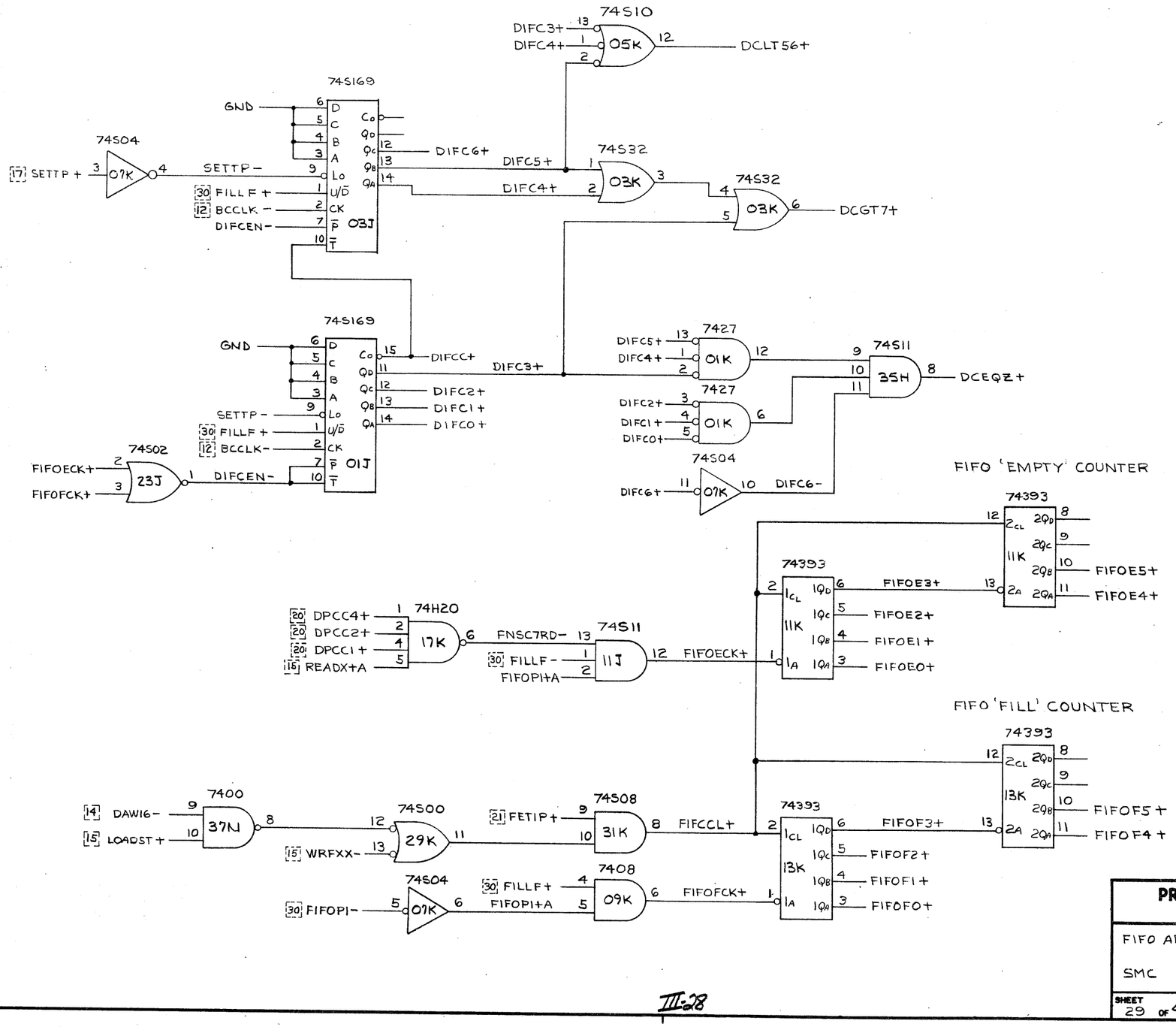
PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
FIFO BUFFER			
SMC 4004		E.V.	
SHEET 28 OF 41	SIZE C	DWG. NO. LBD2702	REV. A

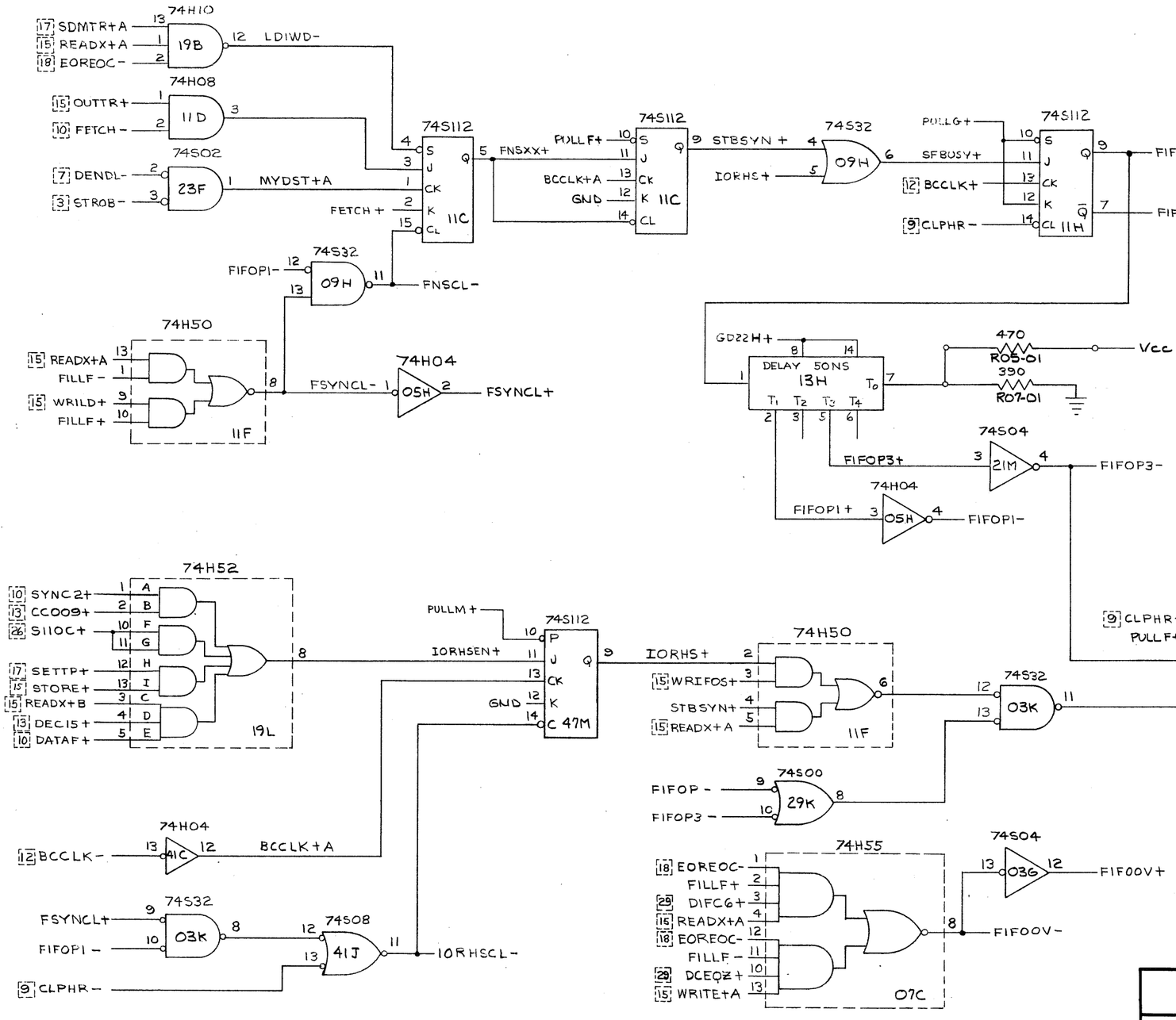
2-74

PDF-003



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
FIFO ADDRESS AND DIFFERENCE LOGIC			
SMC 4004 E.V.			
SHEET 29 OF 41	SIZE C	DWG. NO. LBD 2902	REV A

PDF-003



PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

FIFO CONTROL LOGIC

SMC 4004 E.V.

SHEET	SIZE	DWG. NO.	REV.
30 OF 41	C	LBD2702	A

PDF-003

RECORD ADDRESS REGISTER

74393

[9] CLPHR+ → 12 2CL 2QD 8 → RAD01+
2QC 9 → RAD02+
27J 2QB 10 → RAD03+
13 2A 2QA 11 → RAD04+

74393

[9] CLPHR+ → 2 1CL 1QD 6 → RAD05+
1QC 5 → RAD06+
27J 1QB 4 → RAD07+
[10] HEADCRC+ → 1 1A 1QA 3 → RAD08+

74LS157

RAD01+ → 2 1A 1Y 4 → SADM1+
[14] DAW01+ → 3 1B
RAD02+ → 5 2A 2Y 7 → SADM2+
[14] DAW02+ → 6 2B
RAD03+ → 11 3A 3Y 9 → SADM3+
[14] DAW03+ → 10 3B
RAD04+ → 14 4A 4Y 12 → SADM4+
[14] DAW04+ → 13 4B
[15] DATRN+B → 1 SEL B
GND → 15 G 29J

74LS157

RAD05+ → 2 1A 1Y 4 → SADM5+
[14] DAW05+ → 3 1B
RAD06+ → 5 2A 2Y 7 → SADM6+
[14] DAW06+ → 6 2B
RAD07+ → 11 3A 3Y 9 → SADM7+
[14] DAW07+ → 10 3B
RAD08+ → 14 4A 4Y 12 → SADM8+
[14] DAW08+ → 13 4B
[15] DATRN+B → 1 SEL B
GND → 15 G 31J

RECORD NUMBER COUNTER

74H04

1 → 2IE → 2 → RNCCO-

74161

[14] DAW01- → 6 D CO 15 → RNCCO+
[14] DAW02- → 5 C QD 11 → RNC128+
[14] DAW03- → 4 B QC 12
[14] DAW04- → 3 A QB 13
[10] SETUP- → 9 LO QA 14
[10] FETCH- → 1 CL
2 CK
10 T 41G
7 P

74161

[14] DAW05- → 6 D CO 15 → RNCCX+
[14] DAW06- → 5 C QD 11
[14] DAW07- → 4 B QC 12
[14] DAW08- → 3 A QB 13
[10] SETUP- → 9 LO QA 14
[10] FETCH- → 1 CL
RNCCK- → 2 CK
PULLE+ → 10 T 43G
7 P

74H50

[10] ADDMARK+ → 9 10
[39] TAGEN+ → 13
[15] FORMAT+ → 1
8 → 25J

7474

PULLM+ → 4 S
2 D Q 5
[35] INDEX+ → 3 CK
Q 6
[33] WENXX+ → 1 C 39M

7474

PULLM+ → 10 S
12 D Q 9
11 CK
Q 8
13 C 39M

74S112

PULLM+ → 4 S
TWOIND+ → 3 J Q 5 → INDSYN+
[12] BCCLK+ → 1 CK
GND → 2 K Q 6
[10] WAITX+ → 15 C 47M

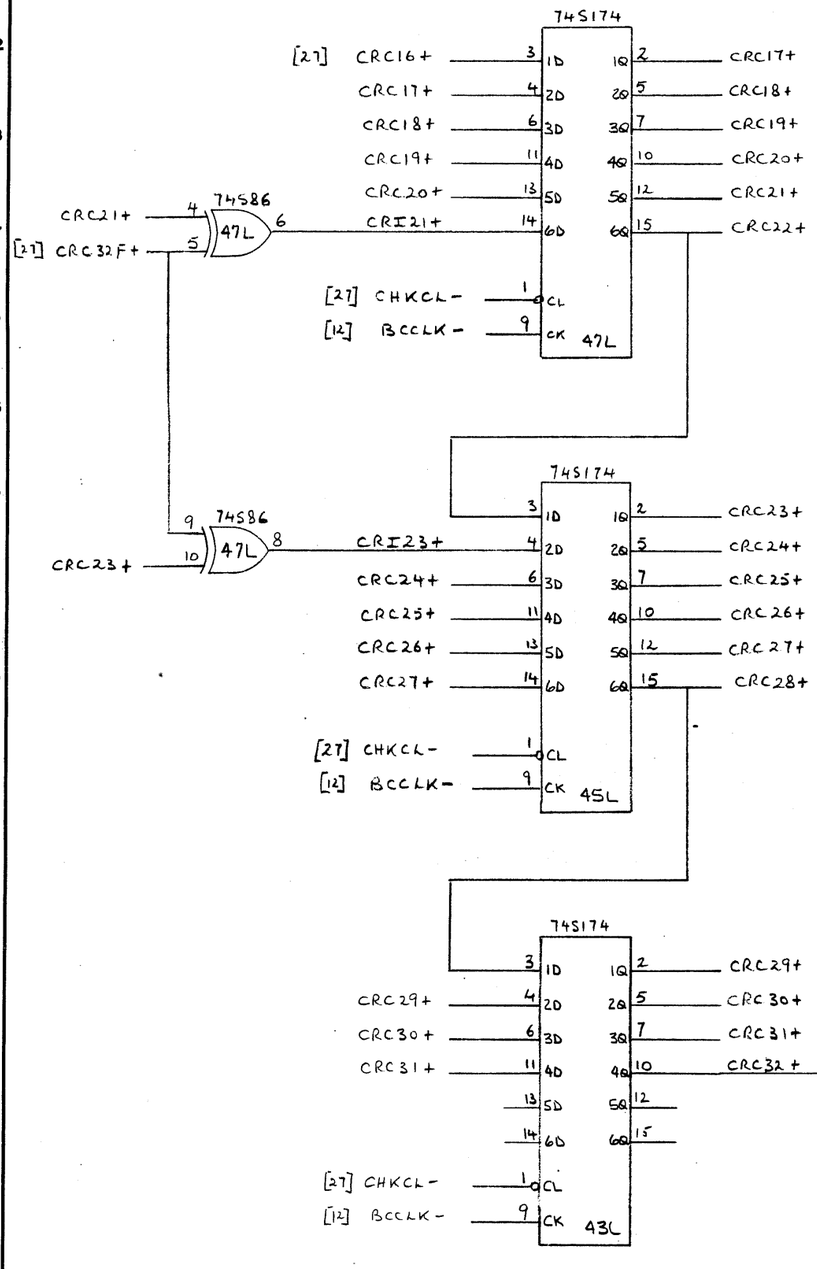
PDF-003

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

DOUBLE INDEX AND RECORD ADDRESS LOGIC

SMC 4004 E.V.

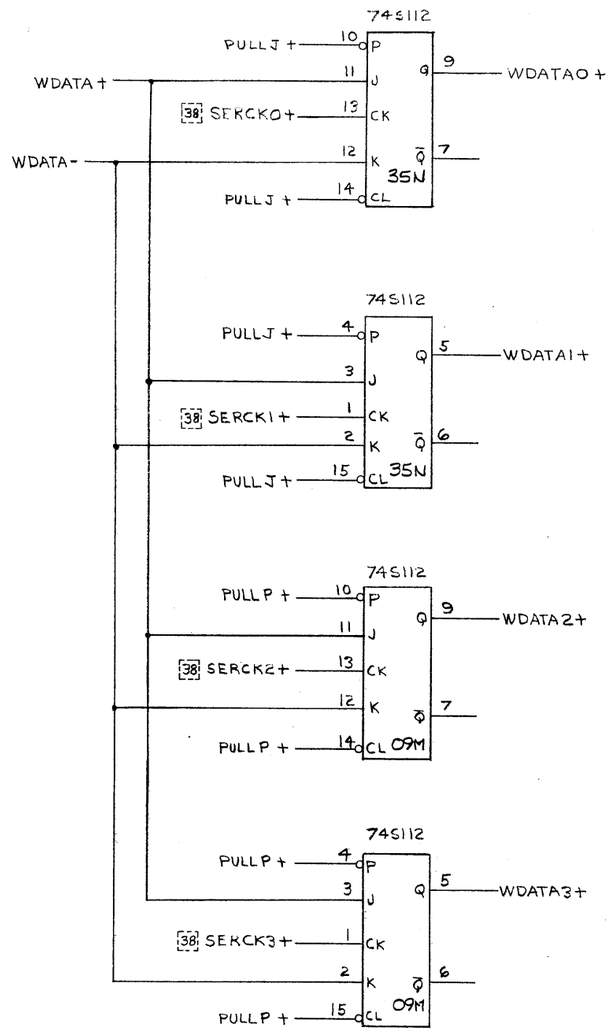
SHEET 31 OF 41 | SIZE C | DWG. NO. LBD 2902 | REV A

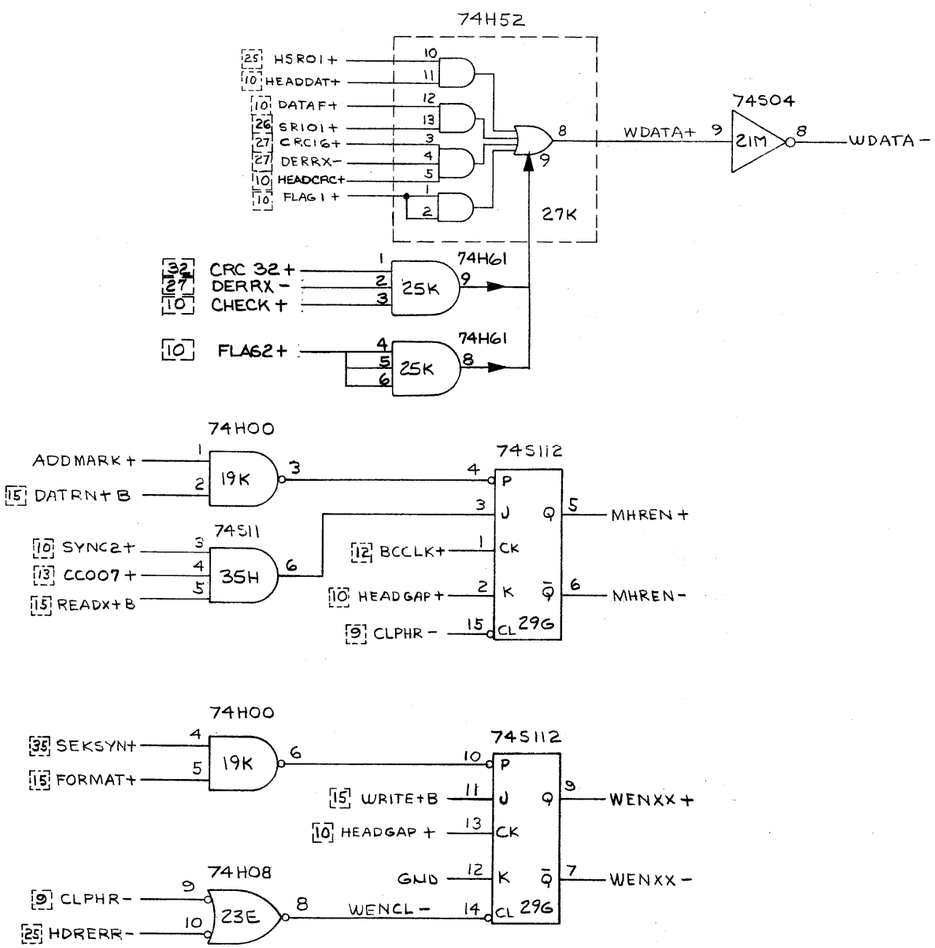


PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
CHECK REGISTER (RIGHT)			
SMC 4004 E.V.			
SHEET 32 OF 41	SIZE C	DWG. NO. LBD2702	REV. A

PDF-003

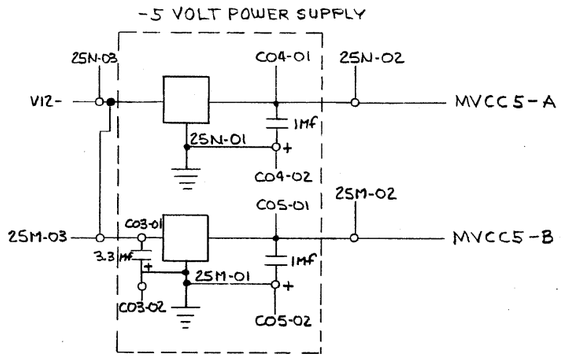
III-31

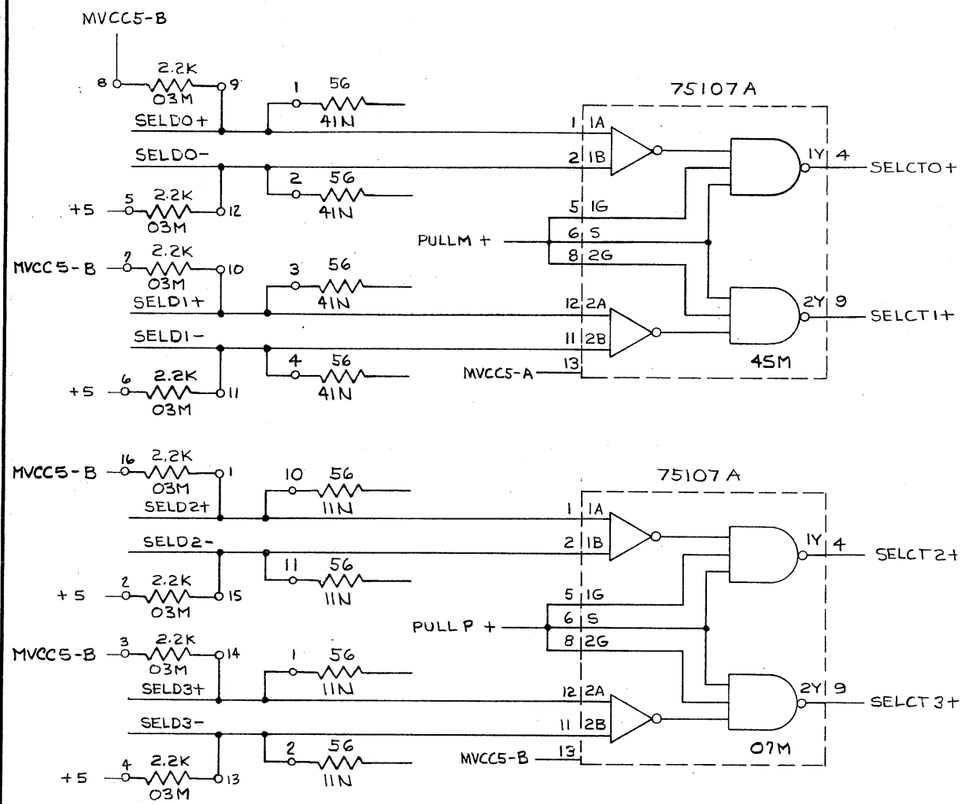


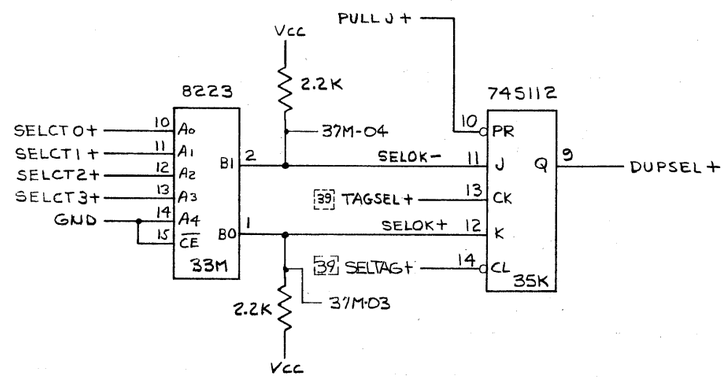


PDF-003

PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
DATA CONTROL			
SMC 4004 E.V.			
SHEET 33 OF 41	SIZE C	DWG. NO. LBD 2902	REV A







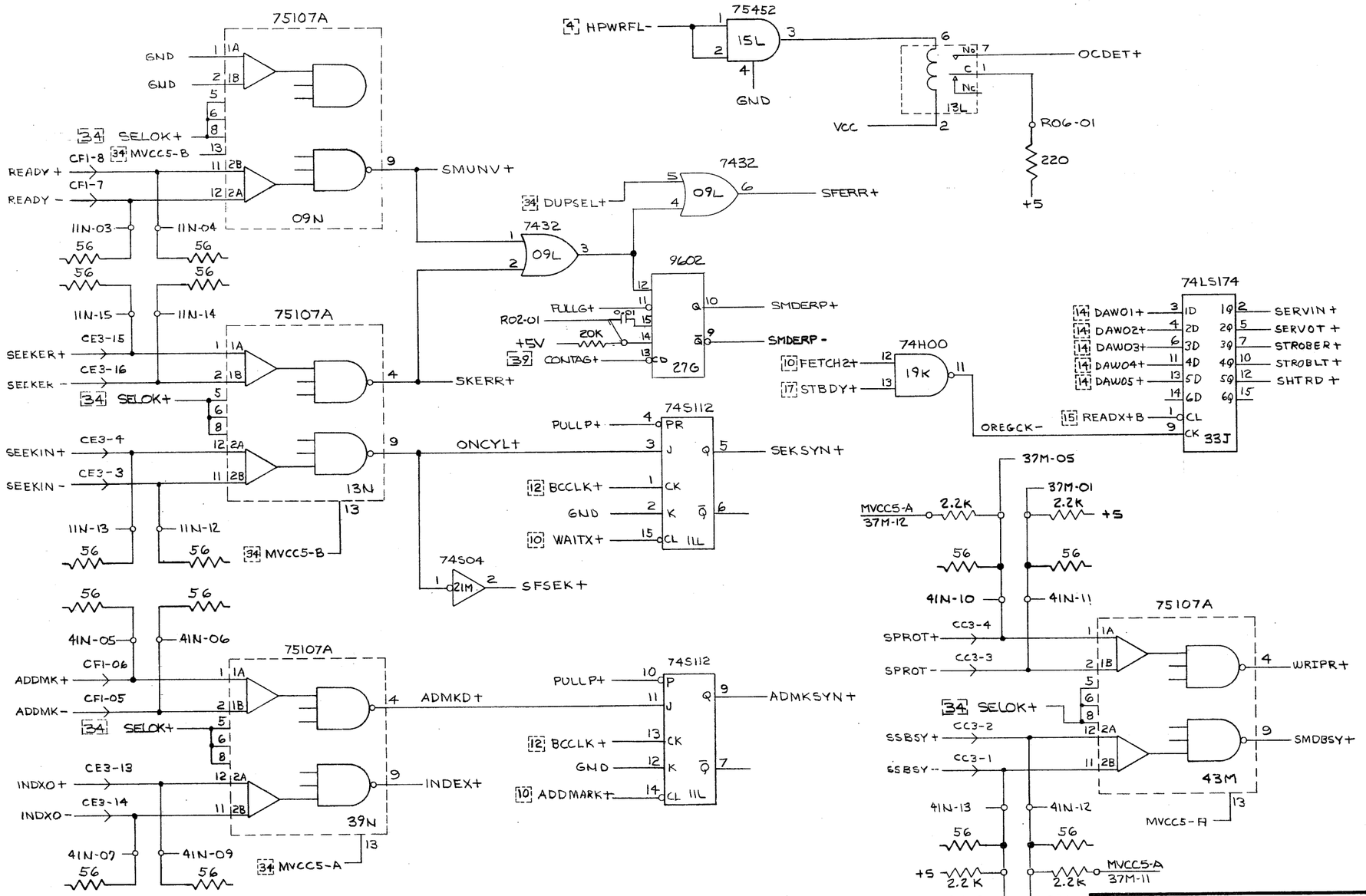
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

DEVICE SELECT LOGIC

SMC 4004 E.V.

SHEET	SIZE	DWG. NO.	REV.
34 OF 41	C	LBD 2702	A

PDF-003



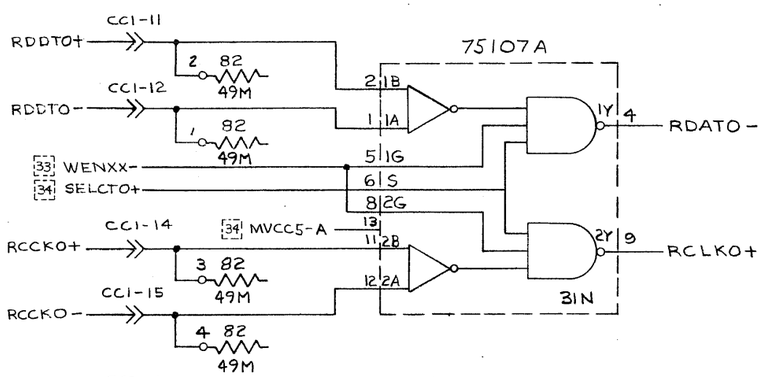
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

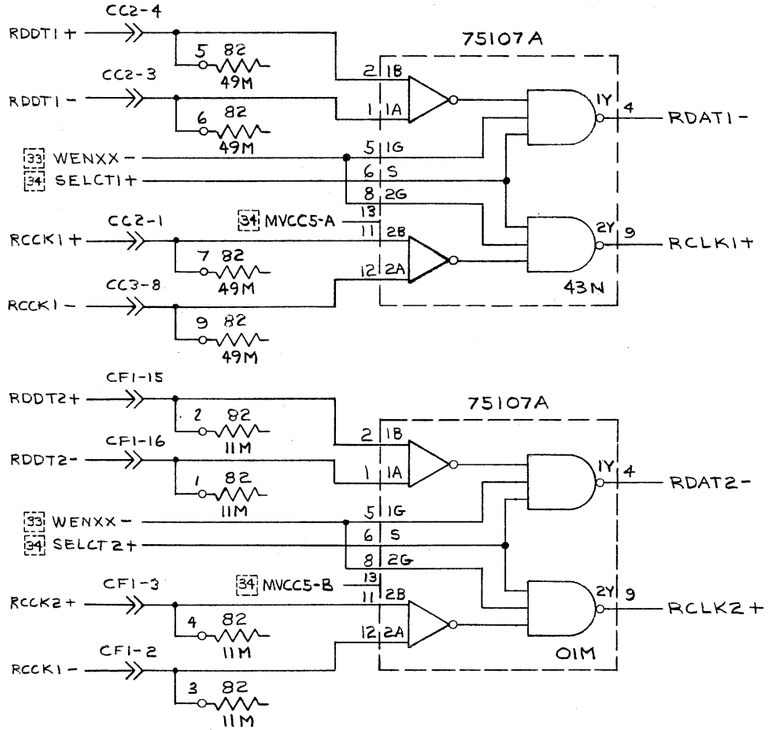
MISC. SMD SIGNALS AND OFFSET

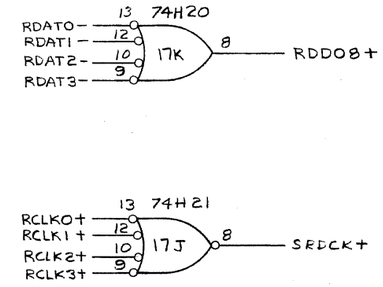
SMC 4004 E.V.

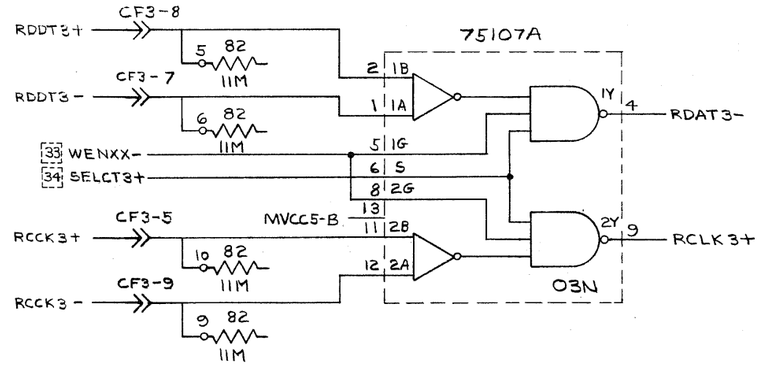
SHEET	SIZE	DWG. NO.	REV
35 OF 41	C	LBD2902	A

PDF-003









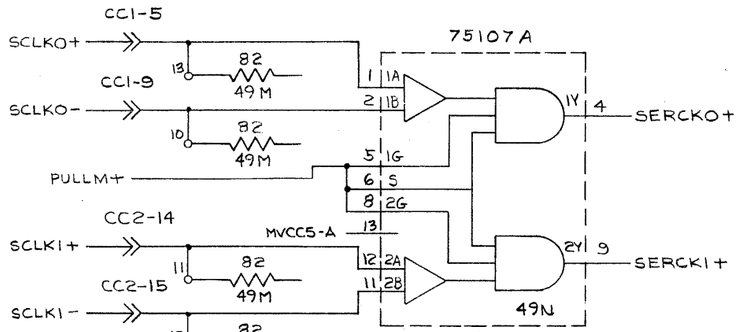
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

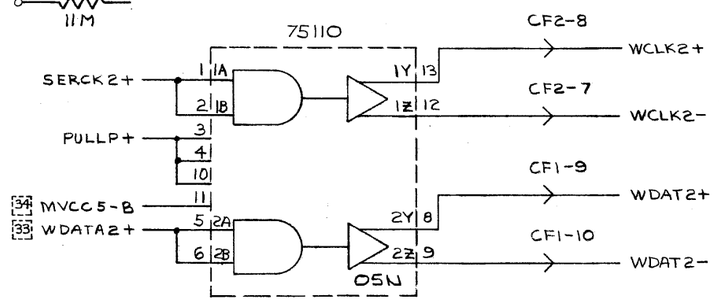
READ DATA AND CLOCK FROM SMD

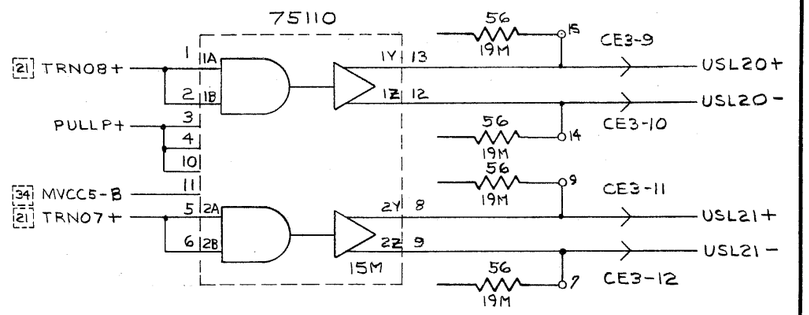
SMC 4004 E.V.

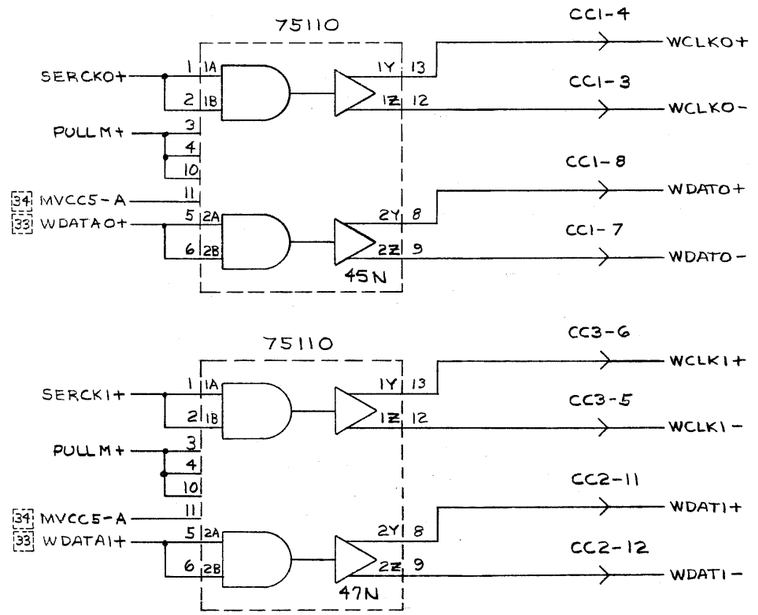
SHEET	SIZE	DWG. NO.	REV.
33 OF 41	C	LBD 2702	A

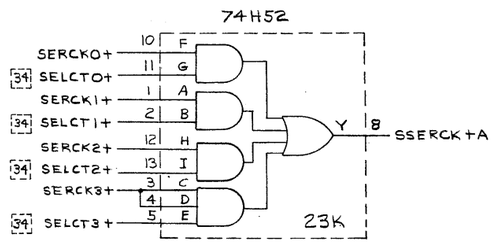
PDF-003











PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

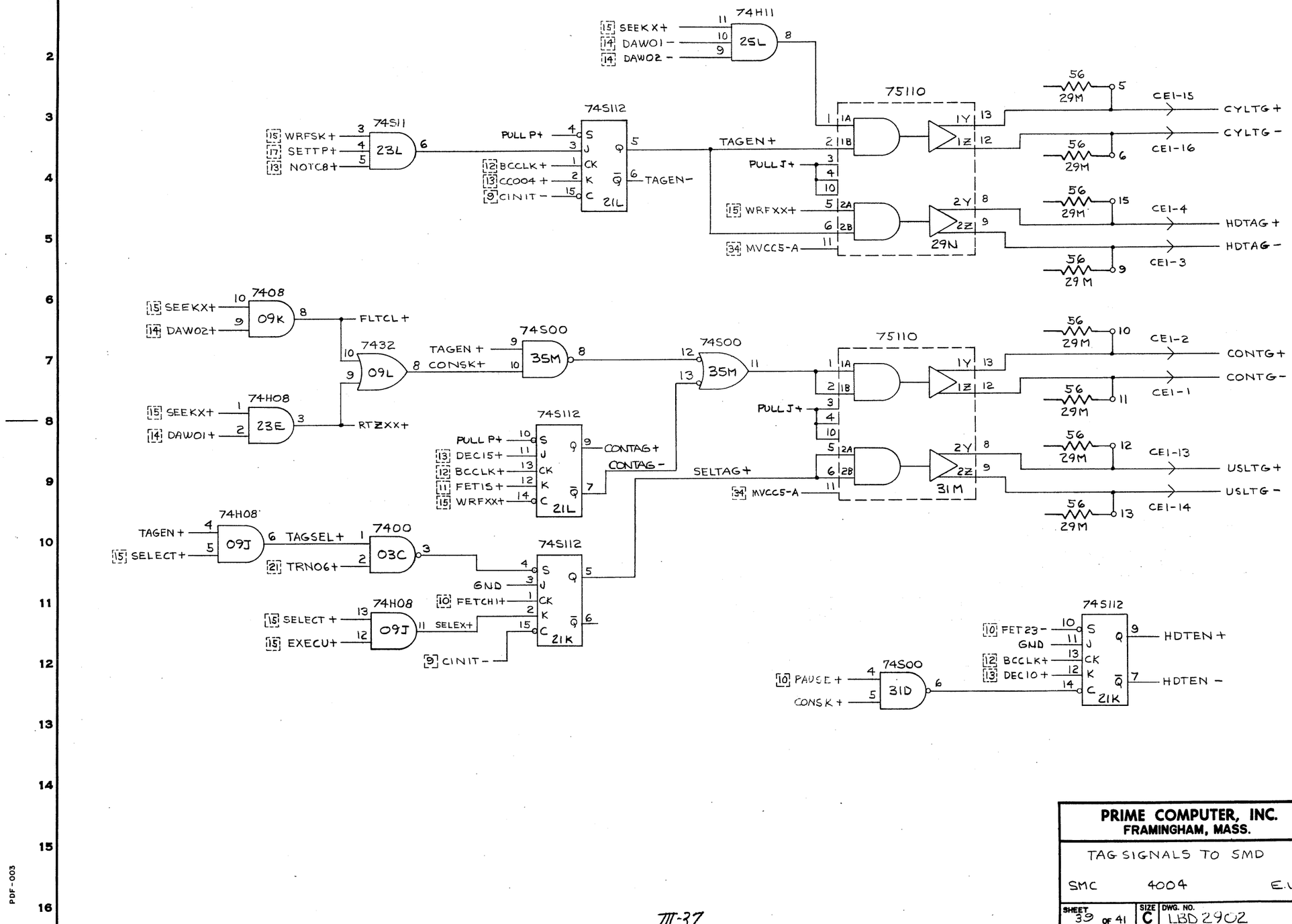
SERVO AND WRITE CLOCK

SMC 4004 E.V

SHEET	SIZE	DWG. NO.	REV.
38 OF 41	C	LBD 2702	A

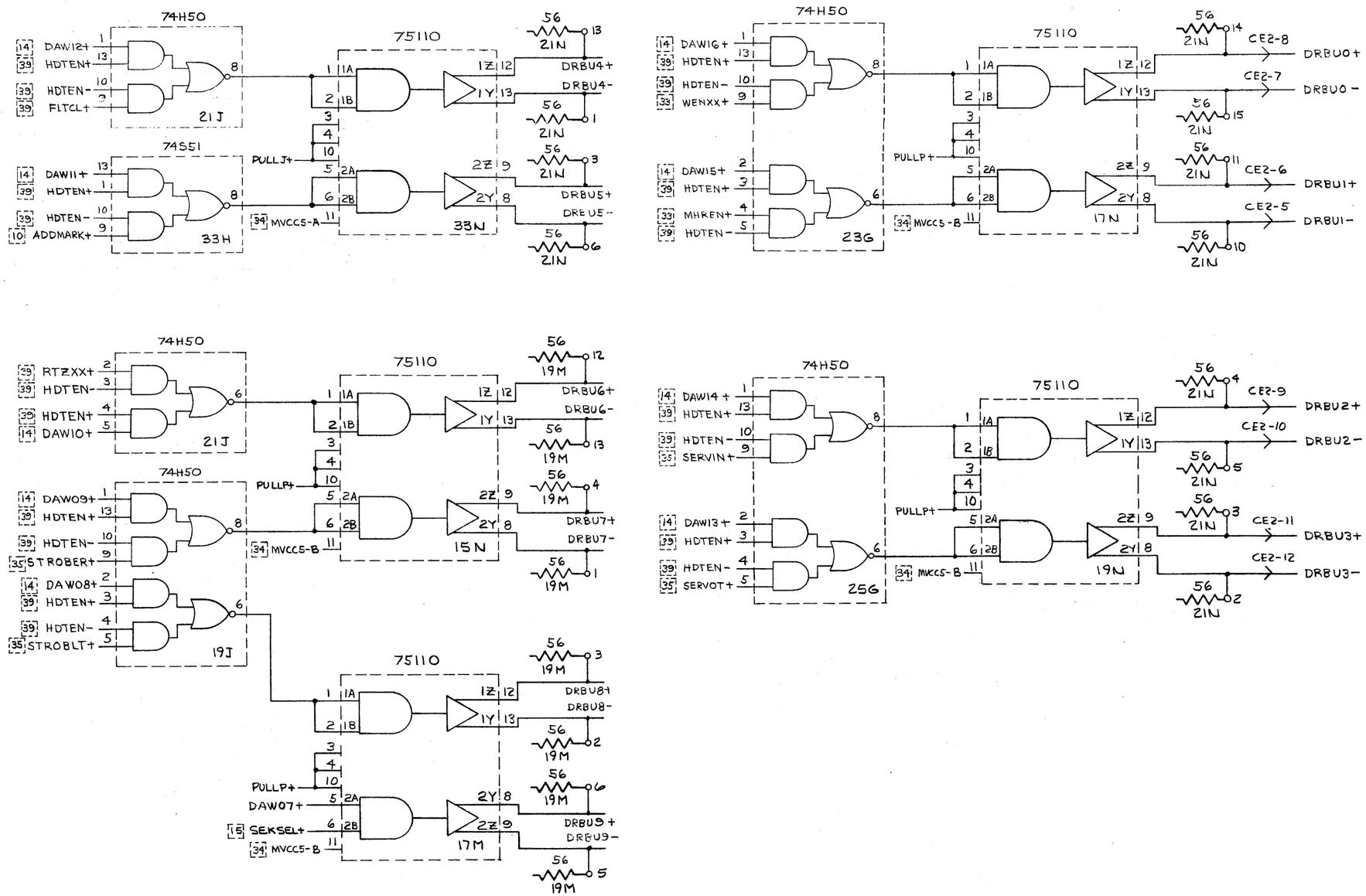
PDF-003

III 36



PRIME COMPUTER, INC. FRAMINGHAM, MASS.			
TAG SIGNALS TO SMD			
SMC	4004		E.V.
SHEET 39 OF 41	SIZE C	DWG. NO. LBD2902	REV. A

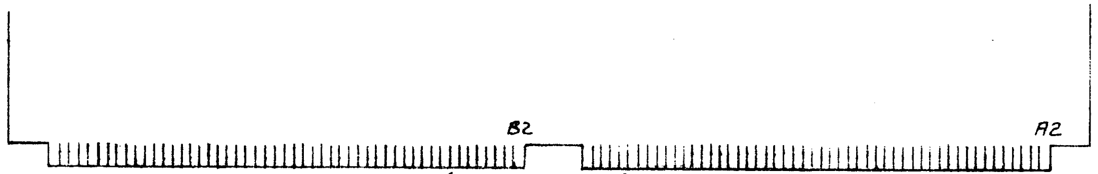
PDF-003



PRIME COMPUTER, INC.	
FRAMINGHAM, MASS.	
BUS SIGNALS TO SMD	
SMC 4004	E.V.
SHEET 40 OF 41	SIZE C / DWG. NO. LBD2902 / REV. A

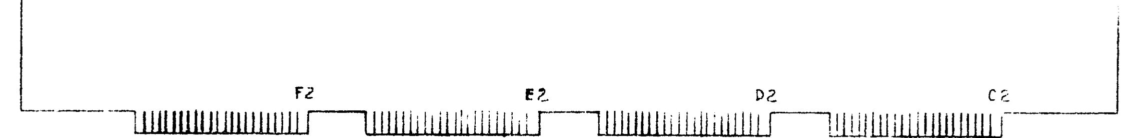
PDF-003

LTR	DATE	REVISION



(SOLDER SIDE)

NAME		CONN PIN	NAME		CONN PIN	NAME		CONN PIN	NAME		CONN PIN
VCC1		CA-1	BMCADL +		CA-51	VCC1		CB-1	BPA12 +		CB-51
VCC1		CA-2			CA-52	VCC1		CB-2	BPA13 +		CB-52
SHIELD(GND)		CA-3			CA-53	GND		CB-3	BPA14 +		CB-53
BPCDCPN+		CA-4			CA-54	TSO(SPARE)		CB-4	BPA15 +		CB-54
BPCDEN +		CA-5			CA-55	BMA99 -		CB-5	BPA16 +		CB-55
GND		CA-6	BMAPEL +		CA-56	BMA00 -		CB-6	BPALP +		CB-56
BPCDPNO -		CA-7	BMAPER +		CA-57	BMA01 -		CB-7	GND		CB-57
BPCDPNA -		CA-8	BMDPEL -		CA-58	BMA02 -		CB-8	BPARP +		CB-58
BPCDPNB -		CA-9	BMDPER -		CA-59	BMA03 -		CB-9	BPCPIO +		CB-59
BPCDPNC -		CA-10	GND		CA-60	BMA04 -		CB-10	BPAPER -		CB-60
BPCDPND -		CA-11	BMD01 +		CA-61	BMA05 -		CB-11	BPCGOCY+		CB-61
BPCDPNE -		CA-12	BMD02 +		CA-62	BMA06 -		CB-12	BPCREDY -		CB-62
BPCDPNF -		CA-13	BMD03 +		CA-63	BMA07 -		CB-13	BPDLP +		CB-63
BPCDPNG -		CA-14	BMD04 +		CA-64	BMA08 -		CB-14			CB-64
BPCDPNH -		CA-15	BMD05 +		CA-65	BMA09 -		CB-15	BPD01 +		CB-65
BPCIEN +		CA-16	BMD06 +		CA-66	BMA10 -		CB-16	BPDRP +		CB-66
BPCIPNO -		CA-17	BMD07 +		CA-67	BMA11 -		CB-17	BPD02 +		CB-67
BPCIPNA -		CA-18	BMD08 +		CA-68	BMA12 -		CB-18	BPD03 +		CB-68
BPCIPNB -		CA-19	BMD09 +		CA-69	BMA13 -		CB-19	BPD04 +		CB-69
BPCIPNC -		CA-20	BMD10 +		CA-70	BMA14 -		CB-20	BPD05 +		CB-70
BPCIPND -		CA-21	BMD11 +		CA-71	BMA15 -		CB-21	BPD06 +		CB-71
SHIELD(GND)		CA-22	BMD12 +		CA-72	BMA16 -		CB-22	BPD07 +		CB-72
BPCICPN +		CA-23	BMD13 +		CA-73	BMALP -		CB-23	BPD08 +		CB-73
GND		CA-24	BMD14 +		CA-74	BMARP -		CB-24	BPD09 +		CB-74
BPCCHI +		CA-25	BMD15 +		CA-75	HPWRFL -		CB-25	BPD10 +		CB-75
SHIELD(GND)		CA-26	BMD16 +		CA-76	GND		CB-26	BPD11 +		CB-76
		CA-27	BMDLP -		CA-77	VCORE1		CB-27	V12 -		CB-77
		CA-28	BMDRP -		CA-78	VCORE1		CB-28	V12 -		CB-78
		CA-29	BMCSELC -		CA-79	BPA01 +		CB-29	BPD12 +		CB-79
BPCEOR +		CA-30	GND		CA-80	GND		CB-30	GND		CB-80
		CA-31	BMCSELB -		CA-81	BPA02 +		CB-31	BPD13 +		CB-81
		CA-32	BMCSELV -		CA-82	BPA03 +		CB-32	BPD14 +		CB-82
		CA-33	BMCDINH -		CA-83	BPA04 +		CB-33	BPD15 +		CB-83
		CA-34	BMCWRS -		CA-84	BPA05 +		CB-34	BPD16 +		CB-84
		CA-35	BMCWLB -		CA-85	BPA06 +		CB-35	BPCMOD0+		CB-85
		CA-36	BMCRFSH -		CA-86	BPA07 +		CB-36	BPCMOD1+		CB-86
		CA-37	BMCEXS1 -		CA-87	BPA08 +		CB-37	BPCMOD2+		CB-87
BPCIDVI -		CA-38	BMCWSTRB -		CA-88	BPA09 +		CB-38	BPCMOD3+		CB-88
		CA-39	BMCEXS2 -		CA-89	BPA10 +		CB-39	BPCINMAD+		CB-89
		CA-40	BPCFCLK +		CA-90	BPA11 +		CB-40	BPCSCLK +		CB-90
		CA-41	BMCSS01 -		CA-91	HSYSCLR -		CB-41	V12 +		CB-91
GND		CA-42	BPCIRQ -		CA-92	GND		CB-42	V12 +		CB-92
BMCWDLR+		CA-43	BMCSS02 -		CA-93	VCORE2		CB-43	HRUN -		CB-93
		CA-44	BPCDRQ -		CA-94	VCORE2		CB-44	HRUN -		CB-94
		CA-45	BMCSS03 -		CA-95	BPDPEL -		CB-45	BPCSTRB +		CB-95
		CA-46	BMCPRCH -		CA-96	GND		CB-46	GND		CB-96
BMCWDLL +		CA-47	BMCCNBL -		CA-97	BPDPER -		CB-47	VSS		CB-97
SHIELD(GND)		CA-48	GND		CA-98	BPAPEL -		CB-48	VSS		CB-98
VCC1		CA-49	VCC2		CA-99	BPA99 +		CB-49	VBB		CB-99
VCC1		CA-50	VCC2		CA-100	BPA00 +		CB-50	VBB		CB-100



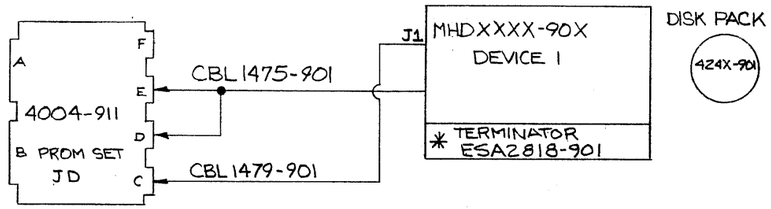
(SOLDER SIDE)

NAME		CONN PIN	NAME		CONN PIN	NAME		CONN PIN	NAME		CONN PIN
WDAT0 +		CC-1	SPROT +		CD-1	USLTG +		CE-1	WDAT2 +		CF-1
WDAT0 -		CC-2	SPROT -		CD-2	USLTG -		CE-2	WDAT2 -		CF-2
GND		CC-3	SSBSY +		CD-3	CYLTG +		CE-3	GND		CF-3
SCLK0 +		CC-4	SSBSY -		CD-4	CYLTG -		CE-4	SCLK2 +		CF-4
SCLK0 -		CC-5			CD-5	HDTAG +		CE-5	SCLK2 -		CF-5
GND		CC-6			CD-6	HDTAG -		CE-6	GND		CF-6
RDDT0 +		CC-7			CD-7	CONTG +		CE-7	RDDT2 +		CF-7
RDDT0 -		CC-8			CD-8	CONTG -		CE-8	RDDT2 -		CF-8
GND		CC-9			CD-9	DRBU0 +		CE-9	GND		CF-9
RCCK0 +		CC-10			CD-10	DRBU0 -		CE-10	RCCK2 +		CF-10
RCCK0 -		CC-11			CD-11	DRBU1 +		CE-11	RCCK2 -		CF-11
GND		CC-12			CD-12	DRBU1 -		CE-12	GND		CF-12
WCLK0 +		CC-13			CD-13	DRBU2 +		CE-13	WCLK2 +		CF-13
WCLK0 -		CC-14			CD-14	DRBU2 -		CE-14	WCLK2 -		CF-14
GND		CC-15			CD-15	DRBU3 +		CE-15	GND		CF-15
		CC-16			CD-16	DRBU3 -		CE-16			CF-16
		CC-17			CD-17	DRBU4 +		CE-17			CF-17
		CC-18			CD-18	DRBU4 -		CE-18			CF-18
		CC-19			CD-19	DRBU5 +		CE-19			CF-19
SELD0 +		CC-20			CD-20	DRBU5 -		CE-20	SELD2 +		CF-20
SELD0 -		CC-21			CD-21	DRBU6 +		CE-21	SELD2 -		CF-21
		CC-22			CD-22	DRBU6 -		CE-22			CF-22
WDAT1 +		CC-23			CD-23	DRBU7 +		CE-23	WDAT3 +		CF-23
WDAT1 -		CC-24			CD-24	DRBU7 -		CE-24	WDAT3 -		CF-24
GND		CC-25			CD-25	DRBU8 +		CE-25	GND		CF-25
SCLK1 +		CC-26			CD-26	DRBU8 -		CE-26	SCLK3 +		CF-26
SCLK1 -		CC-27			CD-27	DRBU9 +		CE-27	SCLK3 -		CF-27
GND		CC-28			CD-28	DRBU9 -		CE-28	GND		CF-28
RDDT1 +		CC-29			CD-29	USL20 +		CE-29	RDDT3 +		CF-29
RDDT1 -		CC-30			CD-30	USL20 -		CE-30	RDDT3 -		CF-30
GND		CC-31			CD-31	USL21 +		CE-31	GND		CF-31
RCCK1 +		CC-32			CD-32	USL21 -		CE-32	RCCK3 +		CF-32
RCCK1 -		CC-33			CD-33	INDX0 +		CE-33	RCCK3 -		CF-33
GND		CC-34			CD-34	INDX0 -		CE-34	GND		CF-34
WCLK1 +		CC-35			CD-35	SEEKER +		CE-35	WCLK3 +		CF-35
WCLK1 -		CC-36			CD-36	SEEKER -		CE-36	WCLK3 -		CF-36
GND		CC-37			CD-37	SEEKIN +		CE-37	GND		CF-37
		CC-38			CD-38	SEEKIN -		CE-38			CF-38
		CC-39			CD-39	OCDET +		CE-39			CF-39
		CC-40			CD-40	GND		CE-40			CF-40
		CC-41			CD-41	READY +		CE-41			CF-41
SELD1 +		CC-42			CD-42	READY -		CE-42	SELD3 +		CF-42
SELD1 -		CC-43			CD-43	ADDMK +		CE-43	SELD3 -		CF-43
		CC-44			CD-44	ADDMK -		CE-44			CF-44

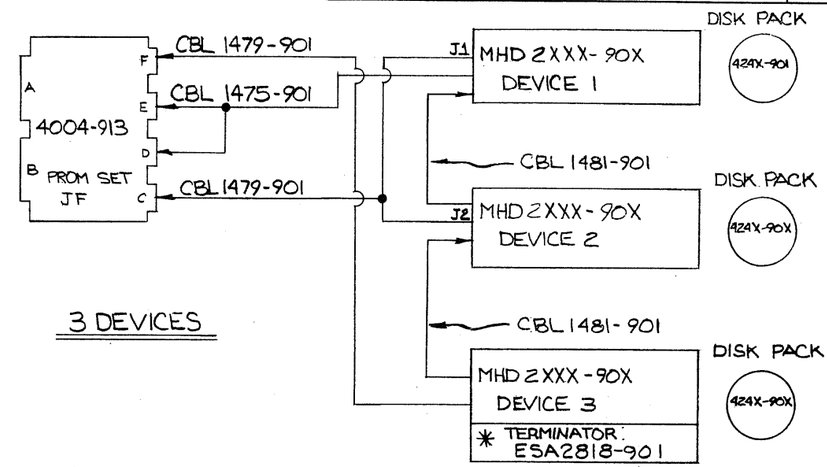
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED – REMOVE ALL BURRS AND SHARP EDGES: – DIMENSIONS ARE IN INCHES – TOLERANCES XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	CONNECTOR SIGNAL NAME LIST
	APPRD	SMC 4004
	USED ON	SCALE
	NEXT ASSY	SHT 41 OF 41 — REV A

M	LTR	DATE	REVISION	DR.	CK.
	A	9/16/76	RELEASED SEE ECR 1898 (CBL 1475-901 REV B)		
	B	12-30-76	REVISED PER ECR 1928		
	C	3-21-77	REVISED PER ECR 2137		

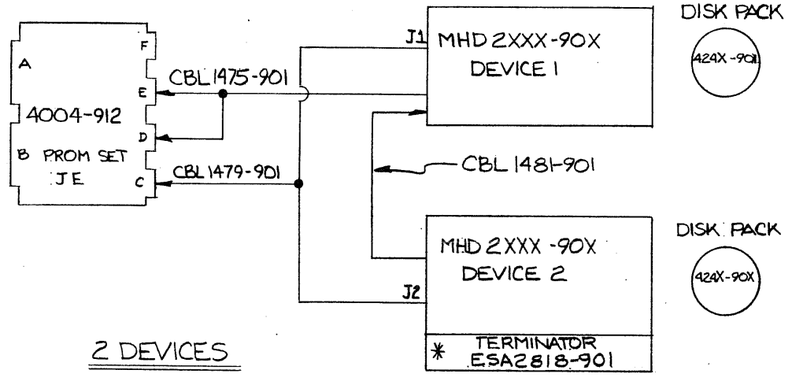
4240 -XXX OR 4242-XXX



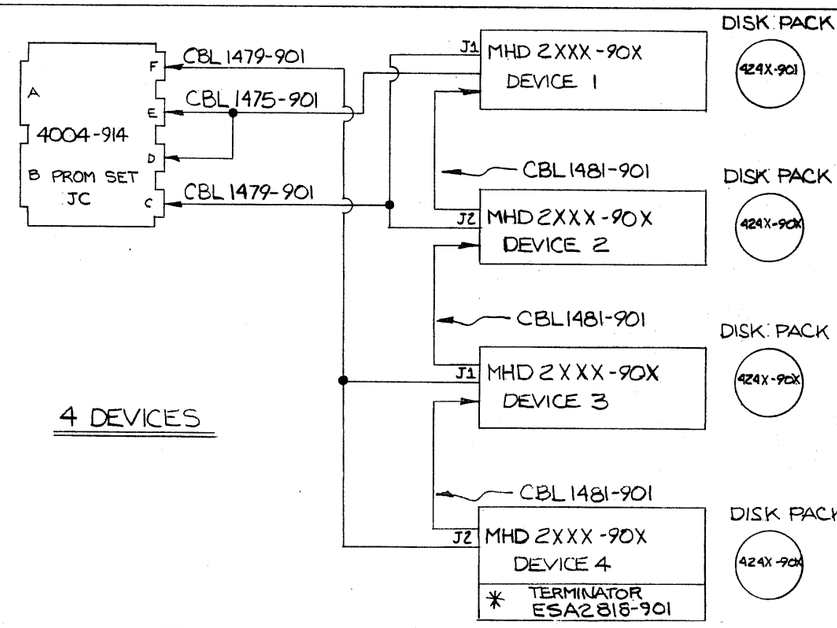
1 DEVICE



3 DEVICES



2 DEVICES



4 DEVICES

NOTES

* 1. TERMINATOR IS TO BE INSTALLED ON LAST DEVICE IN EACH SYSTEM.
2. 80MB & 300MB MHD MAY BE INTERMIXED IN ANY SYSTEM OF TWO OR MORE DEVICES.

PART NUMBER	DESCRIPTION	DISK PACK
MHD2871-902	40 MB MHD 50HZ	4245-901
MHD2871-901	40 MB MHD 60 HZ	
MHD2613-902	300MB MHD 50HZ	4247-901
MHD2613-901	300 MB MHD 60 HZ	
MHD2553-902	80 MB MHD 50HZ	4246-901
MHD2553-901	80 MB MHD 60HZ	

MATERIAL

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN J.F.TRAVALINI 6-14-76
CHK M. Bojan 7-12-76
ENG. Derek Gaudette 9-22-76
APPRD H.W. Mahler 9-16-76
USED ON
NEXT ASSY 4240/41/42/43

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

STORAGE MODULE SYSTEM CONFIGURATION

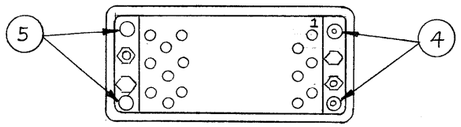
SCALE
SIZE C
DWG. NO. CCD2639-001
REV. C
SHEET 1 OF 1

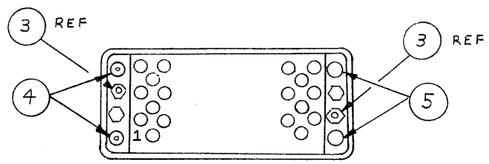
DWG. NO. CCD2639-001 REV. C

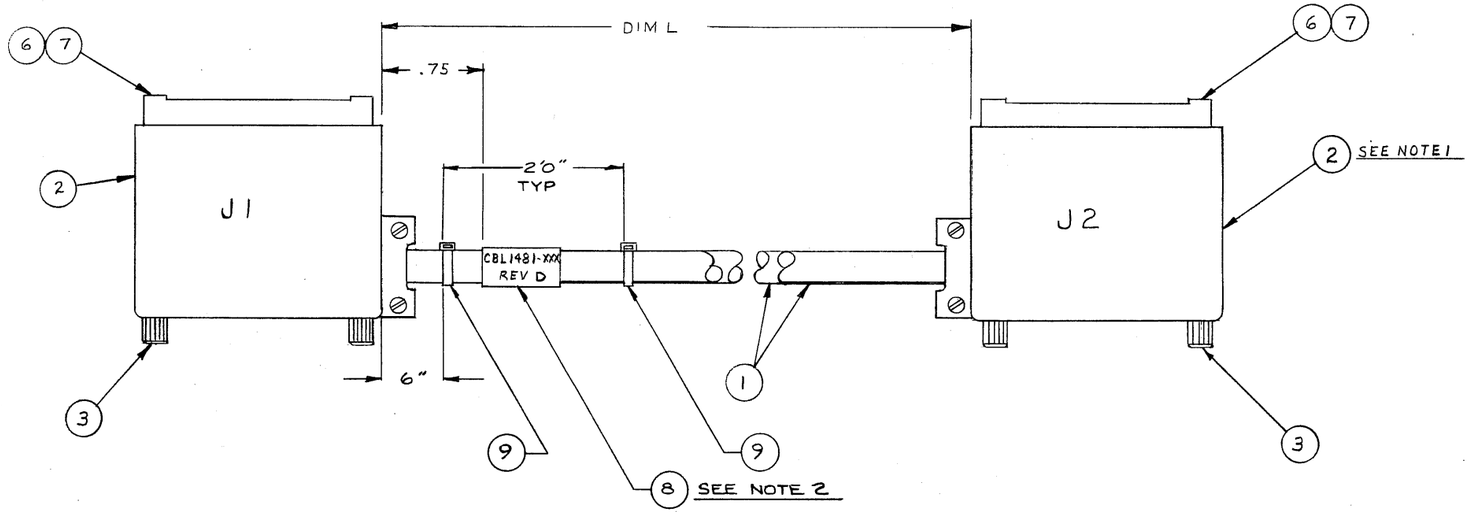
IV-01

WIRE LIST			COMMENTS
FROM	TO	COLOR	
J1-22	J2-22	BLK	TP
J1-25	J2-25	WHT	
J1-46	J2-46	YEL	
J1-49	J2-49	ORG	
J1-48	J2-48	GRN	
J1-51	J2-51	GRY	
J1-52	J2-52	BLK WHT	
J1-55	J2-55	BLK RED	
J1-23	J2-23	BLK GRN	
J1-26	J2-26	BLK ORG	
J1-24	J2-24	BLK YEL	
J1-27	J2-27	BLK BLU	
J1-28	J2-28	WHT BLK	
J1-31	J2-31	WHT RED	
J1-29	J2-29	WHT GRN	
J1-32	J2-32	WHT ORG	
J1-30	J2-30	WHT BLU	
J1-33	J2-33	WHT YEL	
J1-34	J2-34	WHT BRN	
J1-37	J2-37	WHT GRY	
J1-35	J2-35	YEL BLK	
J1-38	J2-38	YEL RED	
J1-36	J2-36	YEL GRN	
J1-39	J2-39	YEL BLU	
J1-40	J2-40	YEL BRN	
J1-43	J2-43	YEL GRY	
J1-41	J2-41	ORG BLK	
J1-44	J2-44	ORG RED	
J1-01	J2-01	ORG GRN	
J1-04	J2-04	ORG BLU	
J1-02	J2-02	ORG BRN	
J1-05	J2-05	ORG GRY	
J1-10	J2-10	GRN BLK	
J1-13	J2-13	GRN RED	
J1-75	J2-75	GRN WHT	
J1-78	J2-78	GRN BLU	
J1-15	J2-15	GRN BRN	
J1-18	J2-18	GRN YEL	
J1-16	J2-16	GRN GRY	
J1-20	J2-20	GRY BLK	
J1-17	J2-17	GRY RED	
J1-21	J2-21	GRY WHT	
J1-42	J2-42	GRY YEL	
J1-45	J2-45	GRY ORG	
J1-56	J2-56	BLK	
J1-53	J2-53	WHT	
J1-50 ⚠B	J2-50 ⚠B	YEL	
J1-47 ⚠B	J2-47 ⚠B	ORG	
J1-76	J2-76	GRN	
J1-73	J2-73	GRY	
J1-77	J2-77	BLK WHT	
J1-74	J2-74	BLK RED	
J1-14	J2-14	BLK GRN	TP ⚠C
J1-11	J2-11	BLK ORG	

M	LTR	DATE	REVISION	DR.	CK.
	A	1/22/76	RELEASED	JPW	JPW
	B	9-9-76	PER ECR 1898	GHT	JTG
	C	11/17/76	ON WIRE LIST, J1-74 WAS J1-44 & J2-74 WAS J2-44, CHANGED PER ECR 1976	GHT	JPW
	D	1-17-77	ON WIRE LIST J1-50 WAS J1-69 J2-50 WAS J2-69 J1-47 WAS J1-54 J2-47 WAS J2-54 PER ECR 2023	JPW	JTG







NOTES:
1. STAMP MARKINGS J1 & J2 .19 HIGH IN BLACK INK LOCATE APPROX AS SHOWN.
2. TYPE PART NO. & REVISION IN BLACK ON ITEM 8 AS SHOWN.
3. CUT OFF UNUSED WIRES AND TERMINATE INSIDE CABLE BOTH ENDS.

DASH NO.	DIM L
-901	10' ± 6"

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN W. Bogan 12/17/75
CHK L.B. McAlarney 12/17/75
ENG. Dave Gardner 12/22/76
APPRD H.W. Nibbs 9-16-76
USED ON
NEXT ASSY 4241-901

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CABLE, DAISY CHAIN (SMD)

SCALE NONE | SIZE C | DWG. NO. CBL1481-XXX | REV D
SHEET 1 OF 1

DWG. NO. CBL1481-XXX REV D

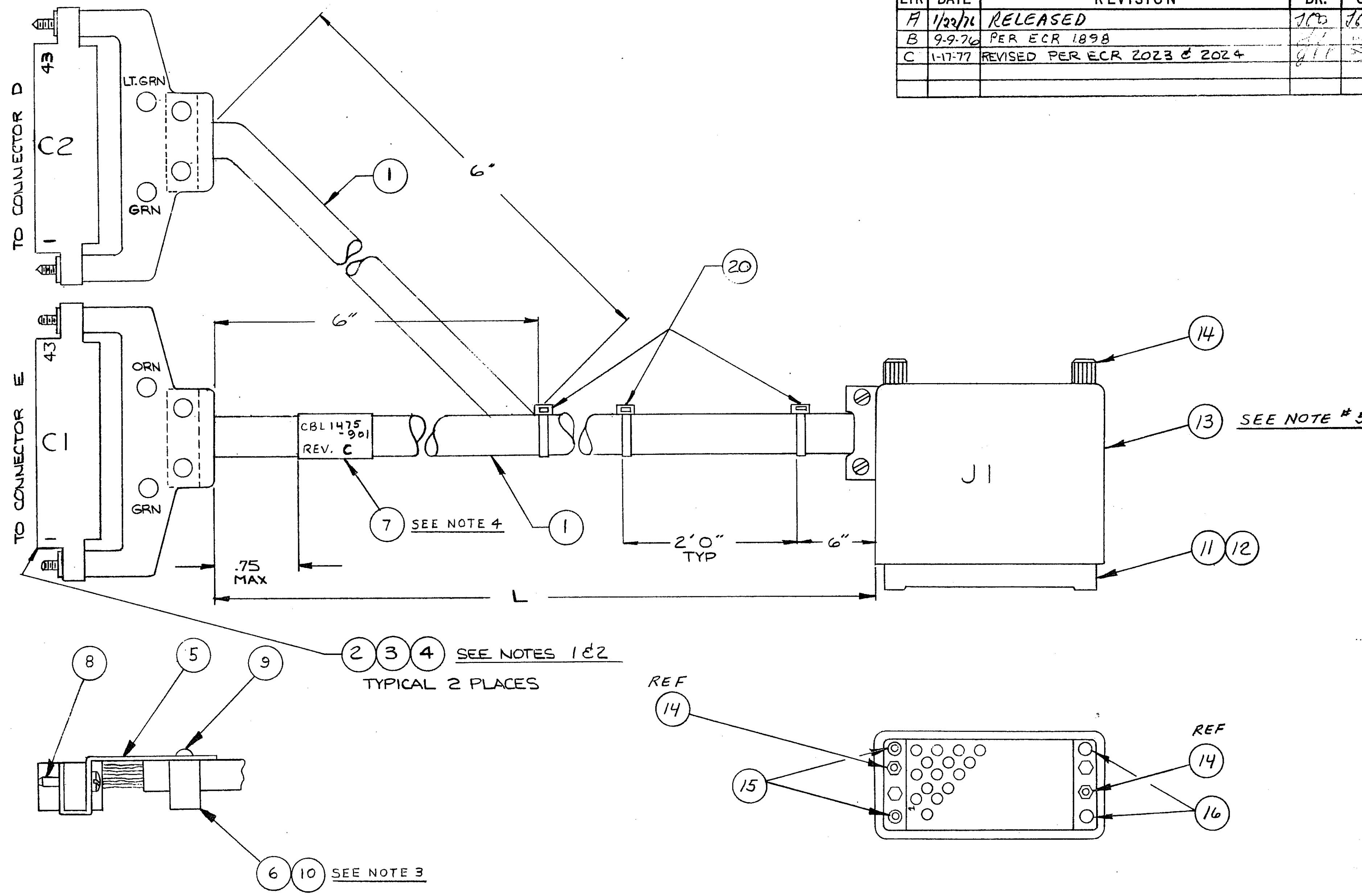
III-02

ER-2

LTR	DATE	REVISION	DR.	CK.
A	1/22/76	RELEASED		
B	9-9-76	PER ECR 1898		
C	1-17-77	REVISED PER ECR 2023 & 2024		

WIRE LIST

FROM	TO	BASE COLOR	STRIPE COLOR	COMMENTS
C1-01	J1-25	BLK	—	TP
C1-02	J1-22	WHT	—	
C1-03	J1-49	YEL	—	
C1-04	J1-46	ORG	—	
C1-05	J1-51	GRN	—	
C1-06	J1-48	GRY	—	
C1-07	J1-55	BLK	WHT	
C1-08	J1-52	BLK	RED	
C1-09	J1-26	BLK	GRN	
C1-10	J1-23	BLK	ORG	
C1-11	J1-27	BLK	YEL	
C1-12	J1-24	BLK	BLUE	
C1-13	J1-31	WHT	BLK	
C1-14	J1-28	WHT	RED	
C1-15	J1-32	WHT	GRN	
C1-16	J1-29	WHT	ORG	
C1-17	J1-33	WHT	BLUE	
C1-18	J1-30	WHT	YEL	
C1-19	J1-37	WHT	BRWN	
C1-20	J1-34	WHT	GRY	
C1-21	J1-38	YEL	BLK	
C1-22	J1-35	YEL	RED	
C1-23	J1-39	YEL	GRN	
C1-24	J1-36	YEL	BLUE	
C1-25	J1-43	YEL	BRWN	
C1-26	J1-40	YEL	GRY	
C1-27	J1-44	ORG	BLK	
C1-28	J1-41	ORG	RED	
C1-29	J1-04	ORG	GRN	
C1-30	J1-01	ORG	BLUE	
C1-31	J1-05	ORG	BRWN	
C1-32	J1-02	ORG	GRY	
C1-33	J1-13	GRN	BLK	
C1-34	J1-10	GRN	RED	
C1-35	J1-78	GRN	WHT	
C1-36	J1-75	GRN	BLUE	
C1-37	J1-18	GRN	BRWN	
C1-38	J1-15	GRN	YEL	
C1-39	J1-20	GRN	GRY	
C1-40	J1-16	GRY	BLK	
C1-41	J1-21	GRY	RED	
C1-42	J1-17	GRY	WHT	
C1-43	J1-45	GRY	YEL	
C1-44	J1-42	GRY	ORG	
C2-01	J1-56	BLK	—	
C2-02	J1-53	WHT	—	
C2-03	J1-50 (C)	YEL	—	
C2-04	J1-47 (C)	ORG	—	
C2-05	J1-76	GRN	—	
C2-06	J1-73	GRY	—	
C2-07	J1-77	BLK	WHT	
C2-08	J1-74	BLK	RED	
C2-09	J1-14	BLK	GRN	TP
C2-10	J1-11	BLK	ORG	



-901	20' 6"
-XXX	L DIM

NOTES:
1. STAMP MARKING C1-C2 .19 HIGH IN WHITE INK LOCATE APPROX AS SHOWN.
2. INSERT KEY ITEM 4 BETWEEN SLOTS 25/26 & 27/28 OF ITEM 2.
3. INSTALL ITEM 10 IN CUTOUT OF ITEM 6 TO INSURE TIGHT FIT OF CABLE.
4. TYPE PART NO. & REV IN BLACK ON ITEM 7 AS SHOWN.
5. STAMP MARKING J1 .19 HIGH IN BLACK INK LOCATE APPROX AS SHOWN.
6. CUT OFF UNUSED WIRES AND TERMINATE INSIDE CABLE BOTH ENDS.

IV-03

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

DWN: 12/17/75
CHK: 12/17/75
ENG.: 1/21/76
APPRD: 4-16-76
USED ON
NEXT ASSY 4240-901

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE CONTROL (SMD) TO 4004 CONTROLLER

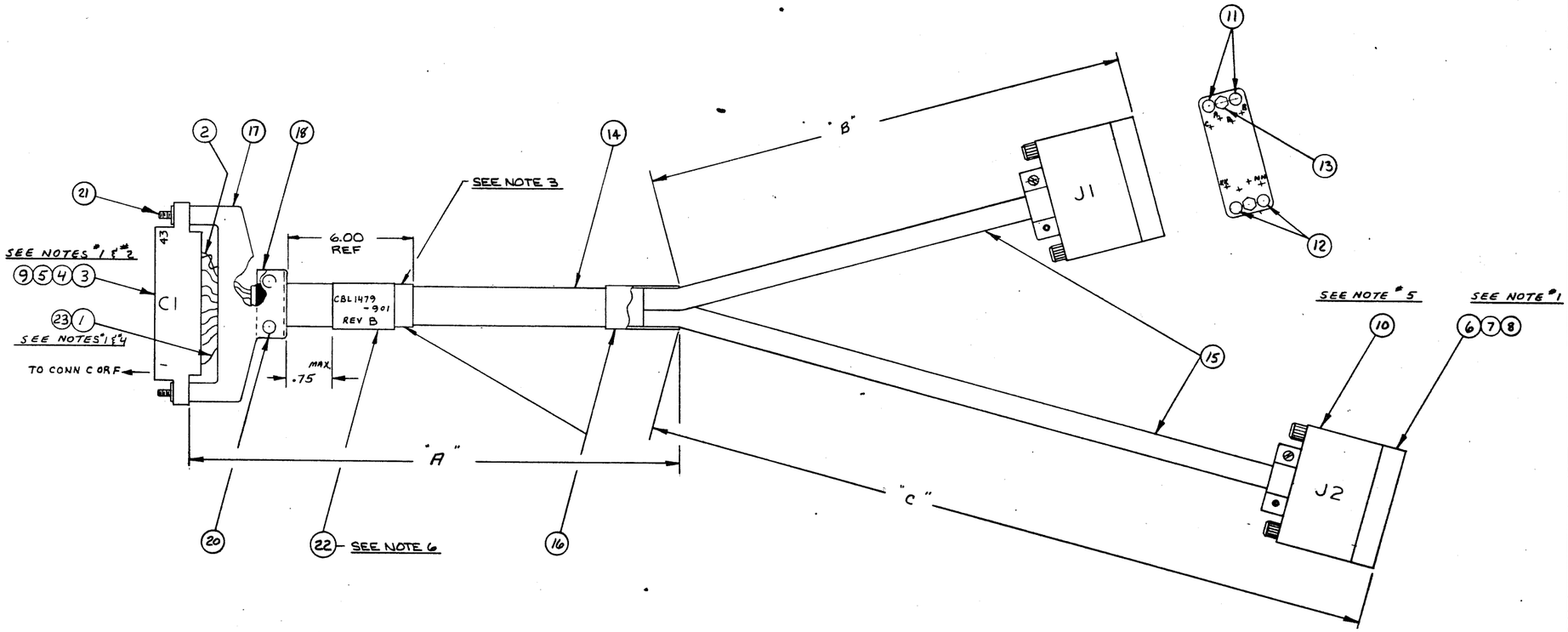
SCALE NONE | SHEET 1 OF 1 | SIZE C | DWG. NO. CBL 1475-XXX | REV C

DWG. NO. CBL 1475-XXX REV. C

WIRE LIST

FROM	TO	COLOR	TYPE OF WIRE	SIGNAL
C1-01	J1-B	BLUE	SHIELDED	WRITE DATA
C1-02	J1-A	WHITE		
C1-03	J1-D	SHIELD*		
C1-04	J1-N	BLUE		SERVO CLOCK
C1-05	J1-M	WHITE		
C1-06	J1-K	SHIELD*		
C1-07	J1-V	BLUE		READ DATA
C1-08	J1-U	WHITE		
C1-09	J1-T	SHIELD*		
C1-10	J1-X	BLUE		READ CLOCK
C1-11	J1-W	WHITE		
C1-12	J1-Y	SHIELD*		
C1-13	J1-J	BLUE	SHIELDED	WRITE CLOCK
C1-14	J1-H	WHITE		
C1-15	J1-E	SHIELD*		
C1-16				
C1-17				
C1-18				
C1-19				
C1-20	J1-BB	RED	TWISTED PAIR	UNIT SELECT
C1-21	J1-DD	BLACK		
C1-22				
C1-23	J2-B	BLUE	SHIELDED	
C1-24	J2-A	WHITE		
C1-25	J2-D	SHIELD*		
C1-26	J2-N	BLUE		
C1-27	J2-M	WHITE		
C1-28	J2-K	SHIELD*		
C1-29	J2-V	BLUE		
C1-30	J2-U	WHITE		
C1-31	J2-T	SHIELD*		
C1-32	J2-X	BLUE		
C1-33	J2-W	WHITE		
C1-34	J2-Y	SHIELD*		
C1-35	J2-J	BLUE	SHIELDED	
C1-36	J2-H	WHITE		
C1-37	J2-E	SHIELD*		
C1-38				
C1-39				
C1-40				
C1-41				
C1-42	J2-BB	RED	TWISTED PAIR	
C1-43	J2-DD	BLACK		

M	LTR	DATE	REVISION	DR.	CK.
	A	1/22/76	RELEASED	JCL	JCL
	B	10-15-76	REVISED PER ECR 1923	JPP	JPP
	C	12/15/76	ITEM 2 WAS ELAN 2. QTY CHANGED ON ITEMS 4,5,7 & 8 PER ECAL 2003-B	K.T.S.	K.T.S.



* 1. SOLDER ONE END OF JUMPER (ITEM # 23) TO BOTH ENDS OF SHIELD OF ITEM # 1 (20 PLACES). CRIMP OTHER END OF JUMPERS TO ITEMS # 5 OR # 8 AS REQ. LENGTH OF JUMPER TO BE DETERMINED BY ASSEMBLER.
2. INSERT ITEM # 9 (KEY) BETWEEN SLOTS 25/26 & 27/28 OF ITEM # 3.
3. ITEM 16 MUST PROTRUDE THRU ITEM 18 TO ASSURE POSITIVE STRAIN RELIEF
4. STAMP MARKINGS C1 IN WHITE INK .19 HIGH. LOCATE APPROX. AS SHOWN.
5. STAMP MARKINGS J1 & J2 IN BLACK INK .19 HIGH. LOCATE APPROX. AS SHOWN.
6. TYPE PART NUMBER & REVISION ON ITEM # 22 AS SHOWN.
7. FOR CABLE CODING LOCATION, SEE DWG INS1210.

-901	10FT. ±6"	10FT. ±6"	15 FT. ±6"
-XXX	DIM. "A"	DIM. "B"	DIM. "C"

IV-04

MATERIAL

UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES.
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02 .XXX ±.005 ANGLES ±1/2°

USED ON
NEXT ASSY

DWN J.C. McQuillan 10/9/75
CHK A. Bogan 1/22/76
ENG. Derek J. Gaudette 1/22/76
APPRD

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CABLE DATA (SMD) TO 4004 CONTROLLER

SCALE NONE | SHEET 1 OF 1 | SIZE D | DWG. NO. CBL1479-XXX | REV. C

CBL1479-XXX C

11-4

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. J.F.P. 12-30-76
CHK. [illegible]
ENG. [illegible] 12/30/77
APPRD. [illegible] 12-30-77

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLER SUB-ASSEMBLY

BOM ESA 2875 **-XXX** REV. D
NHA: 4004-XXX SHT. 1 OF 5

REV.	ECN	CK	REV.	ECN	CK
A	REL 1928	[illegible]			
B	2012	[illegible]			
C	2113	[illegible]			
D	2153	[illegible]			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	ESA2060-901	1								SOCKET ASSY, SMC	
2	C	MEC 0587	1								STIFFENER ASSY	
3	C	MEC 0270	1								PINFIELD GUARD	
4	A	MEC 0412	4								STANDOFF, PINFIELD GUARD	
5		MEC 0309-004	10								SCREW, RD HD NYLON #4-40 X 1/4 LG	
6		MEC 0303-005	5								SCREW, PN HD CRES #4-40 X 5/16 LG	
7		MEC 0388-002	7								NUT, SELF LOCKING #4-40	
8		MEC 0356	5								WASHER, FLAT FIBER #4	
9		MEC 0292	1								PLATE, SERIAL NO.	
10		MEC 2370-001	1								LABEL, ECN LOG	
11		MEC 0303-007	2								SCREW, BD HD #4-40 X 7/16 LG.	
12												
13		MEC 1836-001	2								HEAT SINK, 1 HOLE	
14		MEC 8068-001	A/R								COMPOUND, THERMAL JOINT	
15		CAP 0552-529	2								CAP. TANT 1.0uF 35V ± 10% C1, C2	
16		MEC 0159-001	1'								TUBING, HEAT SHRINK 3/64 ID	
17		MEC 0159-006	3"								TUBING, HEAT SHRINK 1/8 ID	
18		WIR 0542-000	6"								WIRE, 22 AWG STRANDED (BLACK)	
19		WIR 0542-002	2'								WIRE, 22 AWG STRANDED (RED)	
20		WIR 0542-003	6"								WIRE, 22 AWG STRANDED (ORANGE)	
21		WIR 1221-003	2"								WIRE, BUSS #22 AWG	
22		RES 0250-202	1								RESISTOR NETWORK 2K	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. J.F.P. 12-30-76
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLER SUB-ASSEMBLY

BOM ESA2875 **-XXX** REV. D
NHA: SHT. 2 OF 5

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
45		ICD 0040	4								74H53	
46		ICD 0041	3								74H61	
47		ICD 0042	1								74H62	
48		ICD 0043	3								74H74	
49		ICD 0046	1								74H106	
50		ICD 0058	6								7442	
51		ICD 0059	1								8094	
52		ICD 0060	4								8262	
53		ICD 0062	1								9602	
54		ICD 0065	1								75452	
55		ICD 0069	1								7432	
56		ICD 0070	10								74564	
57		ICD 0071	1								74574	
58		ICD 0072	16								745112	
59		ICD 0074	8								745153	
60		ICD 0075	2								745157	
61		ICD 0076	9								745174	
62		ICD 0078	8								745194	
63		ICD 0079	2								82562	
64												
65		ICD 0085	3								74500	
66		ICD 0086	4								74504	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. J.F.P. 12-30-76
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLER SUB-ASSEMBLY

BOM ESA 2875 **-XXX** REV. D
NHA: SHT. 3 OF 5

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
23		RES 0250-153	1								RESISTOR NETWORK 15K	
24		RES 1242-222	1								RESISTOR NETWORK 2.2 K	
25		MEC 1546-001	1								DELAY LINE (DL1)	
26		RES 0250-560	5								RESISTOR NETWORK 56Ω	
27		RES 0250-820	2								RESISTOR NETWORK 82Ω	
28		RES 0250-102	2								RESISTOR NETWORK 1K	
29		MEC 1546-002	1								DELAY LINE (DL2)	
30		REL 1539	1								RELAY, REED SPDT	
31	A	MEC 1721-127	1								RESISTOR CAP ASSY (RC127)	
32		ICD 2486	2								REGULATOR	
33		ICD 0025	5								74H00	
34		ICD 0026	1								74H01	
35		ICD 0027	1								7402	
36		ICD 0028	13								74H04	
37		ICD 0029	6								74H08	1V
38		ICD 0030	4								74H10	
39		ICD 0031	4								74H11	
40		ICD 0033	3								74H20	
41		ICD 0034	3								74H21	
42		ICD 0035	2								74H30	
43		ICD 0038	9								74H50	
44		ICD 0039	8								74H52	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. J.F.P. 12-30-76
CHK.
ENG.
APPRD.

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLER SUB-ASSEMBLY

BOM ESA 2875 **-XXX** REV. D
NHA: SHT. 4 OF 5

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
67		ICD 0088	1								74S10	
68		ICD 0089	4								74S11	
69		ICD 0097	2								74S86	
70		ICD 0112	7								8095	
71												
72		ICD 0191	3								7408	
73		ICD 0194	5								7400	
74		ICD 0195	2								7404	
75		ICD 0196	1								7410	
76		ICD 0201	4								7474	
77		ICD 0215	2								74H55	
78		ICD 0680	1								7427	
79		ICD 2204	2								745169	
80		ICD 2333	3								74S02	
81		ICD 2334	4								74S08	
82		ICD 2336	1								74S20	
83		ICD 2338	6								74S32	
84		ICD 2339	1								74S37	
85		ICD 2345	2								745260	
86		ICD 2346	2								82S09	
87		ICD 2476	4								74166	
88		ICD 2477	3								74393	

PDP-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. JFR 12-30-76 | CHK. | ENG. | APPRD.

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLER SUB-ASSEMBLY

BOM ESA2875 **-XXX** REV. D

NHA: SHT. 5 OF 5

REV.	ECN	CK	REV.	ECN	CK

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
89		ICD 2478	11								74LS157	
90		ICD0052	16								74161	
91		ICD 2480	2								74LS174	
92		ICD 2481	6								74LS175	
93		ICD 2482	3								74S163	
94		ICD 2483	11								75107A	
95		ICD 2484	12								75110	
96		ICD 2340	2								74S51	
97		CAP0130-506	1								CAP. TANT 3.3 uf 35V ± 10%	C3

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. LB 12/30/76 | CHK. JFR | ENG. D. Gardner 1-04-77 | APPRD. W. Mundy 1-25-77

STANDARD COST _____ DATE _____

TITLE: STORAGE MODULE CONTROLLERS SUB-ASSEMBLY

BOM 4004 **-XXX** REV. M

NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
J	1928-A	DF			
K	2012	DF			
L	2113	DF			
M	2153	DF			

ITEM	SIZE	PART NUMBER	QUANTITY -911	-912	-913	-914	-	-	-	DESCRIPTION
1	D	ESA2875-901	1	1	1	1				STORAGE MOD CNTRL SUB ASSY
2	A	MEC1901-056	1	1	1	1				PROM SET JB SMC
3	A	MEC1901-073	-	-	-	1				PROM SET JC SMC
3	A	MEC1901-079	1	-	-	-				PROM SET JD SMC
3	A	MEC1901-080	-	1	-	-				PROM SET JE SMC
3	A	MEC1901-081	-	-	1	-				PROM SET JF SMC
	A	SPC2466	REF							PRODUCT SPEC
	C	LBD2437	REF							LOGIC BLOCK DIAGRAM
	C	CCD2639-001	REF							STORAGE MODULE SYSTEM CONFIGURATION

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. JFR 6/15/76 | CHK. JFR 12/30/76 | ENG. D. Gardner 1-04-77 | APPRD. W. Mundy 12-30-76

STANDARD COST _____ DATE _____

TITLE: DCU, MHD 300MB & DISK PACK 230V 50HZ

BOM 4242-A **-XXX** REV. B

NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	DF			
B	2137	JFR			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	4004-901	1								DCU STORAGE MODULE	
2	C	MHD2613-902	1								MHD 300MB 230V	
3	C	CBL1475-901	1								CABLE, SMD TO 4004	
4	D	CBL1479-901	1								CABLE, 4004 TO CDC S.MOD	
5		4247-901	1								DISK PACK 300MB	
6	C	ESA2818-901	1								STORAGE MODULE TERMINATOR	A
7		MEC0431-001	1								LABEL, PART NUMBER	

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. JFR 6/15/76 | CHK. JFR 12/30/76 | ENG. D. Gardner 1-04-77 | APPRD. W. Mundy 12-30-76

STANDARD COST _____ DATE _____

TITLE: DCU, MHD 300MB & DISK PACK 208V 60HZ

BOM 4242 **-XXX** REV. B

NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	DF			
B	2137	JFR			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	D	4004-901	1								DCU STORAGE MODULE	
2	C	MHD 2613-901	1								MHD, 300MB 208V	
3	C	CBL1475-901	1								CABLE, SMD TO 4004	
4	D	CBL1479-901	1								CABLE, 4004 TO CDC S.MOD	
5		4247-901	1								DISK PACK 300MB	
6	C	ESA2818-901	1								STORAGE MODULE TERMINATOR	A
7		MEC0431-001	1								LABEL, PART NUMBER	
	C	CCD2639-001	REF								S.MODULE SYSTEM CONFIGURATION	

PBF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledoux 3/22/76
CHK. W. Bryan 3/22/76
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: STORAGE MODULE (ADD-ON) DEVICE 50 HZ

BOM 4241-A -XXX REV. C
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	WB			
B	1825	WB			
C	1949	JNT			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	C	MHD2553-902	1	1							80MB STORAGE MODULE 50HZ	A
2	C	CBL1481-901	1	1							CABLE, DAISY CHAIN	
3		4246-901	1	1							DISKPACK, 80MB	A
4		CBL1479-901	–	1							CABLE, DATA-SMD TO 4004	
5	B	CBL2618-901	1	1							CABLE, SAFETY GROUND.	C
		NOTE:										
		4241-A-901	IS	2ND	OR	A	TH	DEVICE	IN		DAISY CHAIN	
		4241-A-902	IS	3RD	DE	VIC	E	IN	DAI	SY	CHAIN	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledoux 3/22/76
CHK. W. Bryan 3/22/76
ENG. Gaudette 3/11/76
APPRD.
STANDARD COST_____ DATE_____

TITLE: STORAGE MODULE SYSTEM 50 HZ (80 MB)

BOM 4240-A -XXX REV. D
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	WB			
B	1825	WB			
C	1949	JNT			
D	2137	JCL			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1		MHD2553-902	1								80MB STORAGE MODULE DISK DRIVE	B
2	C	ESA2818-901	1								STOR. MODULE TERMINATOR	A
3	D	4004-901	1								CONTROLLER (SMC)	
4	C	CBL1475-901	1								CABLE, CONTROL	
5	D	CBL1479-901	1								CABLE, DATA	
6		4246-901	1								DISK PACK 80MB	B
7	B	CBL2618-902	1								CABLE, SAFETY GROUND	C
	C	CCD2639-001	REF								S. MODULE SYSTEM CONFIGURATION	

PDF-004A

PRIME COMPUTER INC.
FRAMINGHAM, MASS.

DWN. Ledoux 3/19/76
CHK. W. Bryan 3/20/76
ENG.
APPRD.
STANDARD COST_____ DATE_____

TITLE: STORAGE MODULE (ADD-ON) DEVICE 60 HZ

BOM 4241 -XXX REV. C
NHA: SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	REL	WB			
B	1825	WB			
C	1949	JNT			

ITEM	SIZE	PART NUMBER	QUANTITY -901	-902	-903	-904	-905	-906	-907	-908	DESCRIPTION	STANDARD COST
1	C	MHD2553-901	1	1							80MB STORAGE MODULE 60HZ	B
2	C	CBL1481-901	1	1							CABLE, DAISY CHAIN	
3		4246-901	1	1							DISKPACK, 80MB	B
4	D	CBL1479-901	–	1							CABLE, DATA-SMD TO 4004	
5	B	CBL2618-901	1	1							CABLE, SAFETY GROUND	C
		NOTE:										
		4241-901	IS	2ND	OR	4TH	DEVICE				IN DAISY CHAIN	
		4241-902	IS	3RD	DEVI	CE	IN	DAISY			CHAIN	

PDF-004A